The first part of the book deals with the design and implementation of “low-voltage low-power data-converters”. The topics have been addressed to the different data-converter topologies, to the different implementation issues (from topology and system level down to circuit level). Moreover the presented solutions have been always analyzed in consideration of the effects of the CMOS technology scaling that reduces device analog performance but offers efficient digital signal processing for analog performance improvement.

In the first paper, Willy Sansen gives an overview of the different ADC topologies, emphasizing the aspects relative to power consumption minimization. This contribution presents a good scenario of the different ADC topologies, like flash (using interpolation & folding), pipeline, SAR and Sigma-Delta, which have been introduced and compared with the data from the implementations most recently reported in literature.

The second paper from Boris Murmann reviews recent developments and low-power design techniques for high-speed pipelined ADC. The fundamental operation principles are introduced, and, then, widely used low-power techniques are summarized. Finally some ideas that have been proposed in recent research publications are outlined.

In the third paper Jan Craninckx discusses the advancements in SAR ADCs design, in particular for wireless transceivers application. An overview is given of recent techniques that reduce the switching power in the capacitive DAC, and as such improve the power ADC efficiency up to levels that are out of reach of the typically used pipeline architecture. Moreover, this paper discusses the charge-sharing SAR ADC architecture, which proposes a new signal processing method in the charge domain that removes the often-neglected though requirements for the reference buffer.

Antonio Digiandomenico et al. propose in the fourth paper low-power large-bandwidth implementations of Continuous-Time Sigma-Delta ADCs, where cascaded architectures and time-encoding signal processing have been successfully applied. Two different implementations, PWM-based and VCO-based, are finally described.
In the fifth paper, Mariam Verhelst et al. discuss digitally-assisted performance enhancement strategies to overcome ADC component mismatch limitation, otherwise addressed by increased component sizes and increased power consumption. Trade-off analysis between mismatch compensation in the analog domain (digitally assisted trimming, possibly in combination with up-scaling) vs. the digital domain (digital post-distortion) is considered. The increasing use of digitally enhanced ADC architectures proves to be the main driver for the observed improvement in area and power with CMOS technology scaling.

Finally the sixth paper from Klaas Bult et al. analyzes the aspects relative to power reduction in very high-frequency DAC. The case study of 12b 2.9 Gs/s DAC is proposed as a benchmark. Several design technique limiting the DAC performances are introduced and eventual solutions are developed.

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