Beginning with this division we enter the field of **sequential circuits**, circuits that have a memorising ability to various degrees. The simplest of these are the **latches**. To understand how memorisation works, we examine it in its elementary form—the latch. Latches prove to be the building blocks of all sequential circuits.

The theory of latches presented in Chap. 9 is general in that it is not restricted to feedback circuits. Most importantly, it contains a **time-independent** definition of a memory function which relies heavily on the concept of **well-behavedness**. It lays the basis for specifying a memory function in a reduced K-map, and for developing evaluation formulas. Chapter 10 applies the time-independent definition of the preceding chapter to **latches with feedback**. Here we discuss the all-important concept of **memorisation hazards**, and how to avoid them: The conventional method being the introduction of an inertial delay in the feedback, the ideal method, on the other hand, being to design the feedback as a **pre-established loop**. When designing latches, minimisation takes a back seat to reliability. Chapter 11 contains a complete discussion of all latches with two inputs and two outputs—the so-called elementary latches—presenting for these a unified set of graphic symbols. Chapter 12 introduces **latch composition**, stating how to realise a given latch on the basis of another. Its theory and application is covered extensively.