Transactions on High-Performance Embedded Architectures and Compilers II
Editor-in-Chief’s Message

It is my pleasure to introduce the second volume of *Transactions on High-Performance Embedded Architectures and Compilers*. This journal was created as an archive for scientific articles in the converging fields of high-performance and embedded computer architectures and compiler systems. Design considerations in both general-purpose and embedded systems are increasingly being based on similar scientific insights. For example, a state-of-the-art game console today consists of a powerful parallel computer whose building blocks are the same as those found in computational clusters for high-performance computing. Moreover, keeping power/energy consumption at a low level for high-performance general-purpose systems as well as in, for example, mobile embedded systems is equally important in order to keep heat dissipation at a manageable level or to maintain a long operating time despite the limited battery capacity. It is clear that similar scientific issues have to be solved to build competitive systems in both segments. Additionally, for high-performance systems to be realized – be it embedded or general-purpose – a holistic design approach has to be taken by factoring in the impact of applications as well as the underlying technology when making design trade-offs. The main topics of this journal reflect this development as follows:

- Processor architecture, e.g., network and security architectures, application specific processors and accelerators, and reconfigurable architectures
- Memory system design
- Power, temperature, performance, and reliability constrained designs
- Evaluation methodologies, program characterization, and analysis techniques
- Compiler techniques for embedded systems, e.g., feedback-directed optimization, dynamic compilation, adaptive execution, continuous profiling/optimization, back-end code generation, and binary translation/optimization
- Code size/memory footprint optimizations

For the second volume of *Transactions on HiPEAC* we received 31 submissions and accepted 15 papers. Ten of these are regular submissions. We also set up a submission server, which has made the submission handling much more convenient for the authors, the reviewers, and the editors. I would like to thank Thomas van Parys and Sylvie Detournay of Ghent University for being instrumental in setting up this precious infrastructure.

This volume contains 15 papers divided into two sections. The first section is a special part containing the top five papers from the Second International Conference on High-Performance Embedded Architectures and Compilers held in Ghent January 28-30, 2007. The second section is a set of ten regular papers. The topics of these general papers are a good pick of the ones covered by the journal, such as microarchitecture, memory systems, code generation, and performance modeling.
The editorial board has worked diligently to handle the papers for the journal. I would like to thank all the contributing authors, editors, and reviewers for their excellent work.

However, one of the editors, a dear colleague and friend, is no longer with us. In April 2007, Professor Stamatis Vassiliadis passed away after a long time of illness. He was a passionate visionary leader for our field, with too many contributions to mention, and was a key person behind the establishment of the HiPEAC Network of Excellence. We miss him immensely as a dear colleague and friend.

I would like to welcome a new member of the editorial board. Dr. Georgi Gaydadjiev is an expert on reconfigurable computing, a field that he as well as Stamatis have contributed to heavily. We welcome Dr. Gaydadjiev aboard!

Per Stenström
Chalmers University of Technology
Editor-in-Chief
Transactions on HiPEAC
Per Stenström is a professor of computer engineering at Chalmers University of Technology. His research interests are devoted to design principles for high-performance and embedded computer systems. He is an author of two textbooks and more than a hundred research publications. He regularly serves program committees of major conferences in the computer architecture field as well as actively contributing to editorial boards. He has been an editor of *IEEE Transactions on Computers* and is an editor of the *Journal of Parallel and Distributed Computing* and the *IEEE Computer Architecture Letters*. Further, he served as the General as well as the Program Chair of the ACM/IEEE Int. Symp. on Computer Architecture, the IEEE Int. Symp. on High-Performance Computer Architecture, the ACM Int. Conf. on Languages, Compilers, and Tools for Embedded Systems, the Int. Conf. on High-Performance Embedded Architectures and Compilers, and the IEEE Int. Parallel and Distributed Processing Symp. He is a member of the ACM and the SIGARCH, a Fellow of the IEEE, and a founding member of the Network of Excellence on High-Performance and Embedded Architecture and Compilation funded by the European Commission under FP6 and FP7.

Koen De Bosschere obtained his PhD from Ghent University in 1992. He is a professor in the ELIS Department at the Universiteit Gent where he teaches courses on computer architecture and operating systems. His current research interests include: computer architecture, system software, code optimization. He has co-authored 150 contributions in the domain of optimization, performance modeling, microarchitecture, and debugging. He is the coordinator of the ACES research network and of the European HiPEAC2 network. He can be contacted at Koen.DeBosschere@elis.UGent.be.
Jose Duato is professor in the Department of Computer Engineering (DISCA) at UPV, Spain. His research interests include interconnection networks and multiprocessor architectures, and he has published over 340 papers. His research results have been used in the design of the Alpha 21364 microprocessor, and the Cray T3E, IBM BlueGene/L, and Cray Black Widow supercomputers. Dr. Duato is the first author of the book *Interconnection Networks: An Engineering Approach*. He served as associate editor of IEEE TPDS and IEEE TC. He was General Co-chair of ICPP 2001, Program Chair of HPCA-10, and Program Co-chair of ICPP 2005. He has also served as Co-chair, Steering Committee member, Vice-Chair, or Program Committee member in more than 55 conferences, including HPCA, ISCA, IPPS/SPDP, IPDPS, ICPP, ICDCS, Europar, and HiPC.

Georgi Gaydadjiev is a professor in the computer engineering laboratory of the Technical University of Delft, The Netherlands. His research interests focus on many aspects of embedded systems design with an emphasis on reconfigurable computing. He has published about 50 papers on this topics in international refereed journals and conferences. He has acted as Program Committee member of many conferences and is subject area editor for the *Journal of Systems Architecture*. 
Manolis Katevenis received his PhD degree from U.C. Berkeley in 1983 and the ACM Doctoral Dissertation Award in 1984 for his thesis on “Reduced Instruction Set Computer Architectures for VLSI.” After a brief term on the faculty of Computer Science at Stanford University, he has been in Greece, with the University of Crete and with FORTH, since 1986. After RISC, his research has been on interconnection networks and interprocessor communication. In packet switch architectures, his contributions since 1987 have been mostly in per-flow queuing, credit-based flow control, congestion management, weighted round-robin scheduling, buffered crossbars, and non-blocking switching fabrics. In multiprocessing and clustering, his contributions since 1993 have been on remote-write-based, protected, user-level communication. His URL is http://archvlsi.ics.forth.gr/~kateveni.

Michael O’Boyle is a professor in the School of Informatics at the University of Edinburgh and an EPSRC Advanced Research Fellow. He received his PhD in Computer Science from the University of Manchester in 1992. He was formerly a SERC Postdoctoral Research Fellow, a Visiting Research Scientist at IRISA/INRIA Rennes, a Visiting Research Fellow at the University of Vienna, and a Visiting Scholar at Stanford University. More recently he was a Visiting Professor at UPC, Barcelona.

Dr. O’Boyle’s main research interests are in adaptive compilation, formal program transformation representations, the compiler impact on embedded systems, compiler directed low-power optimization, and automatic compilation for parallel single-address space architectures. He has published over 50 papers in international journals and conferences in this area and manages the Compiler and Architecture Design group consisting of 18 members.
Cosimo Antonio Prete is full professor of Computer Systems at the University of Pisa, Italy, and faculty member of the PhD School in computer Science and Engineering (IMT), Italy. He is coordinator of the graduate degree program in Computer Engineering and rector’s adviser for Innovative Training Technologies at the University of Pisa. His research interests are focused on multiprocessor architectures, cache memory, performance evaluation, and embedded systems. He is an author of more than 100 papers published in international journals and conference proceedings. He has been project manager for several research projects, including: the SPP project, OMI, Esprit IV; the CCO project, supported by VLSI Technology, Sophia Antipolis; the ChArm project, supported by VLSI Technology, San Jose; and the Esprit III Tracs project.

André Seznec is “directeur de recherches” at IRISA/INRIA. Since 1994, he has been the head of the CAPS (Compiler Architecture for Superscalar and Special-purpose Processors) research team. He has been conducting research on computer architecture for more than 20 years. His research topics have included memory hierarchy, pipeline organization, simultaneous multithreading, and branch prediction. In 1999-2000, he spent his sabbatical with the Alpha Group at Compaq.
Olivier Temam obtained a PhD in computer science from the University of Rennes in 1993. He was assistant professor at the University of Versailles from 1994 to 1999, and then professor at the University of Paris Sud until 2004. Since then, he has been a senior researcher at INRIA Futurs in Paris, where he heads the Alchemy group. His research interests include program optimization, processor architecture, and emerging technologies, with a general emphasis on long-term research.

Theo Ungerer is Chair of Systems and Networking at the University of Augsburg, Germany, and Scientific Director of the Computing Center of the University of Augsburg. He received a Diploma in Mathematics at the Technical University of Berlin in 1981, a Doctoral Degree at the University of Augsburg in 1986, and a second Doctoral Degree (Habilitation) at the University of Augsburg in 1992. Before his current position he was scientific assistant at the University of Augsburg (1982-89 and 1990-92), visiting assistant professor at the University of California, Irvine (1989-90), professor of computer architecture at the University of Jena (1992-1993) and the Technical University of Karlsruhe (1993-2001). He is a Steering Committee member of HiPEAC and of the German Science Foundation’s priority programme on “Organic Computing.” His current research interests are in the areas of embedded processor architectures, embedded real-time systems, organic, bionic, and ubiquitous systems.
Mateo Valero obtained his PhD at UPC in 1980. He is a professor in the Computer Architecture Department at UPC. His research interests focus on high-performance architectures. He has published approximately 400 papers on these topics. He is the director of the Barcelona Supercomputing Center, the National Center of Supercomputing in Spain. Dr. Valero has been honored with several awards, including the King Jaime I by the Generalitat Valenciana, and the Spanish national award “Julio Rey Pastor” for his research on IT technologies. In 2001, he was appointed Fellow of the IEEE, in 2002 Intel Distinguished Research Fellow, and since 2003 he has been a Fellow of the ACM. Since 1994, he has been a foundational member of the Royal Spanish Academy of Engineering. In 2005 he was elected Correspondent Academic of the Spanish Royal Academy of Sciences, and his native town of Alfamén named their public college after him.
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