The second part of this book is dedicated to formal verification methods. It deals with two main topics: logic satisfiability and equivalence checking.

For logic satisfiability, a nontrivial circuit duality between tautology and contradiction check is introduced, which can speed up SAT tools. Also, an alternative Boolean satisfiability framework based on majority logic is proposed. For equivalence checking, a new approach to verify faster the combinational equivalence between two reversible logic circuits is presented.