The on-chip integration of multiple low voltage power supplies is a primary concern in high performance ICs. An integrated power system should deliver high quality power to multiple loads in an energy efficient manner. The load regulation and power efficiency of individual power supplies within a power delivery system are particularly important and affect the overall performance of the power delivery process. The physical size of a power supply is also critical for integrating multiple power supplies on-chip. Several power delivery circuits are described in Part IV.

To provide a high quality power delivery system, the power needs to be regulated on-chip with ultra-small locally distributed power efficient converters. Different types of power supplies are reviewed in Chap. 16. To exploit the advantages of existing power supplies, a heterogeneous power delivery system is described. The power efficiency of the system is shown to be a strong function of the clustering of the power supplies—the specific configuration in which the power converters and regulators are co-designed.

The primary design characteristic that affects the development of multiple on-chip power supplies is the on-chip area. A small hybrid on-chip voltage regulator is described in Chap. 17. This active filter based voltage regulator is a combination of a buck converter and a low dropout (LDO) voltage regulator. The performance of the active filter based regulator is compared with other recently developed on-chip voltage regulators.

A fully integrated power delivery system with distributed on-chip LDO regulators developed for voltage regulation in portable mobile devices is described in Chap. 18. The circuit is fabricated in a 28 nm CMOS process. Each LDO employs adaptive bias for fast and power efficient voltage regulation, exhibiting 0.4 ns response time of the regulation loop and 98.45% current efficiency. An adaptive compensation network is also employed within the distributed power delivery system to maintain a stable system response.

With hundreds of power domains and thousands of cores, DVS and DVFS within each core are primary design objectives for efficiently managing a power budget. In addition, line regulation will become more important when hundreds of power supplies operate together on a single monolithic substrate. Efficient design
techniques and circuits for adaptive control of power lines are therefore important. A digitally controlled current starved pulse width modulator for adaptively changing the voltage of a power converter is described in Chap. 19. Analytic closed-form expressions for the operation of a pulse width modulator are provided. The accuracy and performance of the pulse width modulator is evaluated with 22 nm CMOS predictive technology models under PVT variations. The pulse width modulator is appropriate for dynamic voltage scaling systems due to the small on-chip area and high accuracy under PVT variations.