Decoupling capacitors are an integral element of the power distribution network design process. Different topics related to decoupling capacitance are discussed in Part III. This part is divided into several chapters, discussing strategies for efficiently placing decoupling capacitors within on-chip power distribution network and the co-design of multiple decoupling capacitors with multiple on-chip power supplies. Each of the following chapters is summarized below.

Decoupling capacitance is described in Chap. 11. A historical perspective of capacitance is provided. The decoupling capacitor is shown to be analogous to a reservoir of charge. A hydraulic analogy of the hierarchical placement of decoupling capacitors is also described. It is demonstrated that the impedance of a power distribution system can be maintained below a target specification over an entire range of operating frequencies by utilizing a hierarchy of decoupling capacitors. Antiresonance in the impedance of a power distribution system with decoupling capacitors is also intuitively explained in this chapter. Different types of on-chip decoupling capacitors are compared. Several allocation strategies for placing on-chip decoupling capacitors are reviewed.

On-chip decoupling capacitors have traditionally been allocated into the available free (or white) space on a die. The efficacy of the on-chip decoupling capacitors however depends upon the impedance of the power/ground lines connecting the capacitors to the current loads and power supplies. A design methodology for placing on-chip decoupling capacitors is presented in Chap. 12. The maximum effective radii of an on-chip decoupling capacitor is determined by the target impedance (during discharge) and the charge time. Two criteria to estimate the minimum required on-chip decoupling capacitance are also presented.

As the minimum feature size continues to scale, additional on-chip decoupling capacitance will be required to support increasing current demands. A larger on-chip decoupling capacitance requires a greater area which cannot conveniently be placed close to the switching load circuits. Moreover, a large decoupling capacitor exhibits a distributed impedance behavior. A lumped model of an on-chip decoupling capacitor, therefore, results in underestimating the capacitance requirements, thereby increasing the power noise. A methodology for efficiently
placing on-chip distributed decoupling capacitors is the subject of Chap. 13. Design techniques to estimate the location and magnitude of a system of distributed on-chip decoupling capacitors are presented. Different tradeoffs in the design of a system of distributed on-chip decoupling capacitors are also evaluated.

Multiple decoupling capacitors with multiple on-chip power supplies is the topic of Chap. 14. The large number of on-chip power supplies and decoupling capacitors inserted throughout an integrated circuit complicates the design and analysis of power distribution networks. Complex interactions among the power supplies, decoupling capacitors, and active load circuitry are evaluated utilizing a computationally efficient analysis methodology. The effect of the physical distance among the power supplies and decoupling capacitors on power supply noise is discussed. A design methodology for simultaneously placing the on-chip power supplies and decoupling capacitors is described. This methodology changes conventional practices where the power distribution network is designed first, followed by placing the decoupling capacitors.