The third and final part of the book presents tools and methodologies in High-Performance Reconfigurable Computing, a crucial part of making FPGAs an efficient economic solution for HPC applications. The first chapter is a contribution on precision and arithmetic concerns in HPRC from de Dinechin and Pasca of Ecole Normale Superieure de Lyon, France, and Altera European Technology Center, UK, respectively. The following three contributions are on design tools, starting with a contribution from Schafer and Wakabayashi of NEC Corporation, Japan, which presents a comparison between a C-based high level synthesis (HLS) approach and an RTL-based approach to the discrete element method (DEM). Following this, Perry et al. from Edinburgh Parallel Computing Centre (EPCC), UK, present a benchmarking exercise of Euroben kernels on the Maxwell FPGA supercomputer using a hand-coded VHDL-based approach and a C-based HLS approach. After that, a contribution from El Araby et al. from the Catholic University of America, USA, IBM Corporation, India, and the George Washington University, USA, presents a review and taxonomy of high-level languages (HLLs) for HPRC and a framework for their analysis, with programmer productivity taking centre stage. Indeed, programmer productivity in HPRC has been identified by the community as a major problem which needs to be addressed. This part ends with a contribution from Pell et al. from Maxeler Technologies, UK, and Imperial College London, UK, which presents an integrated approach to HPRC based on a dataflow software framework, and hardware that is optimised to the application in hand.