The second part of the book is concerned with architectural developments in High-Performance Reconfigurable Computing. It starts with a contribution from Klauer of the Helmut Schmidt University, Germany, on Convey computing – one of the most ambitious and pragmatic commercial attempts to bring the power of FPGAs into mainstream computing. This is followed by a contribution from Castillo et al. from Spain which presents an academic effort to build a low cost high performance reconfigurable computer, called SMILE. Next, Baity-Jesi et al. from Spain and Italy present a domain-specific FPGA-based supercomputer used for statistical physics, called Janus.

The following three chapters deal with networking and communications issues in FPGA-based parallel systems. First, Nüssle et al. from the University of Heidelberg, Germany, present an FPGA-based low-latency interconnection network called EXTOLL. Then, Baier et al. from Germany and the USA present an FPGA-based high-speed torus interconnect and its implementation for two parallel machines, namely QPACE and AuroraScience. After that, Fröning et al. from the University of Heidelberg, Germany, and Universitat Politècnica de València, Spain, present an FPGA-based cluster memory architecture which allows for dynamic resource provisioning.

This part ends with a contribution from Minoru Watanabe of Shizuoka University, Japan, which presents a radically novel high performance reconfigurable computing paradigm based on high-speed optical dynamic reconfiguration.