Multiprocessor System-on-Chip
Michael Hübner • Jürgen Becker
Editors

Multiprocessor System-on-Chip

Hardware Design and Tool Integration

Springer
Preface

For the next decade, Moore’s Law is still going to bring higher transistor densities allowing Billions of transistors to be integrated on a single chip. However, it became more and more obvious that exploiting significant amounts of instruction-level parallelism with deeper pipelines and more aggressive wide-issue superscalar techniques, and using most of the transistor budget for large on-chip caches has come to an dead end. Especially, scaling performance with higher clock frequencies is getting more and more difficult because of heat dissipation problems and too high energy consumption. The latter is not only a technical problem for mobile systems, but is even going to become a severe problem for computing centers because high energy consumption leads to significant cost factors in the budget. Improving performance can only be achieved by exploiting parallelism on all system levels.

Therefore, for high-performance computing systems, for high-end servers as well or for embedded systems, a massive paradigm shift towards multicore architectures is taking place. Integrating multiple cores on a single chip leads to a significant performance improvement without increasing the clock frequency. Multicore architectures offer a better performance/Watt ratio than single core architectures with similar performance.

Combining multicore and coprocessor technology promise extreme computing power for highly CPU-time-consuming applications in scientific computing as well as for special purpose applications in the embedded area. Especially FPGA-based accelerators not only offer the opportunity to speedup an application by implementing their compute-intensive kernels into hardware but also to adapt to the dynamical behavior of an application.

The purpose of this book is to evaluate strategies for future system design in MPSoC architectures. Both aspects, hardware design and tool-integration into existing development tools will be discussed. Also the novel trends in MPSoC combined with reconfigurable architectures are a topic in this book. The main emphasis is on architectures, design-flow, tool-development, applications and system design.
We kindly want to thank all authors and co-authors for their excellent contributions which enabled finally the development of this book. Furthermore we want to thank the Springer Team, namely Mrs. Amanda Davis, Mr. Charles Glaser and Ms. Jeya Ruby for their great support and patience.

Karlsruhe, Germany

Jürgen Becker
Michael Hübner
Contents

1 An Introduction to Multi-Core System on Chip – Trends and Challenges ............................................................ 1
   Lionel Torres, Pascal Benoit, Gilles Sassatelli, Michel Robert,
   Fabien Clermidy, and Diego Puschini

Part I “Application Mapping and Communication Infrastructure”

2 Composability and Predictability for Independent Application Development, Verification, and Execution ............ 25
   Benny Akesson, Anca Molnos, Andreas Hansson,
   Jude Ambrose Angelo, and Kees Goossens

3 Hardware Support for Efficient Resource Utilization in Manycore Processor Systems .................................................. 57
   A. Herkersdorf, A. Lankes, M. Meitinger, R. Ohlendorf,
   S. Wallentowitz, T. Wild, and J. Zeppenfeld

4 PALLAS: Mapping Applications onto Manycore .......................... 89
   Michael Anderson, Bryan Catanzaro, Jike Chong, Ekaterina Gonina,
   Kurt Keutzer, Chao-Yue Lai, Mark Murphy, Bor-Yiing Su,
   and Narayanan Sundaram

5 The Case for Message Passing on Many-Core Chips ............... 115
   Rakesh Kumar, Timothy G. Mattson, Gilles Pokam,
   and Rob Van Der Wijngaart
Part II “Reconfigurable Hardware in Multiprocessor Systems”

6 Adaptive Multiprocessor System-on-Chip Architecture:
   New Degrees of Freedom in System Design and Runtime Support ..................................................... 127
   Diana Göhringer, Michael Hübner, and Jürgen Becker

Part III “Physical Design of Multiprocessor Systems”

7 Design Tools and Methods for Chip Physical Design .................. 155
   Ricardo Reis

8 Power-Aware Multicore SoC and NoC Design .................... 167
   Miltos D. Grammatikakis, George Kornaros, and Marcello Coppola

Part IV Trends and Challenges for Multiprocessor Systems

9 Embedded Multicore Systems: Design Challenges and Opportunities ....................................................... 197
   Dac Pham, Jim Holt, and Sanjay Deshpande

10 High-Performance Multiprocessor System on Chip:
    Trends in Chip Architecture for the Mass Market ................... 223
    Rob Aitken, Krisztian Flautner, and John Goodacre

11 Invasive Computing: An Overview ........................................ 241
    Jürgen Teich, Jörg Henkel, Andreas Herkersdorf, Doris Schmitt-Landsiedel, Wolfgang Schröder-Preikschat, and Gregor Snelting

Index ........................................................................... 269