The first chapter of this book is on High-Speed AD Converters. It addresses both generic high-speed design issues and specific design examples. ‘High-speed’ can be interpreted in two ways. It can mean in absolute sense the most high-speed converters, like addressed in the first two papers. However, it can also have a meaning in relative sense: those converters where the speed is dictated by the application, but where the dynamic properties dominate the performance. Depending on the application specifications, several architectures come into the picture. The next four papers address design techniques and design examples, for different type of architectures, that shift the speed barriers towards higher values by alleviating the analog requirements, by correction and calibration in the digital domain, or by giving a better understanding and modeling, thus paving the way to more optimized designs.

The first two papers address design aspects of really high-speed ADCs, with 22GS/s and 20GS/s design examples; these papers include a more general and tutorial like review. The first one, of Peter Schvan, addresses a time-interleaved flash converter, operating at 22GS/s with 5 bit resolution, made in a bipolar technology. Sources of degradation at high speed are discussed before the design is elaborated. Bipolar has for several reasons been the technology of choice for very high-speed converters up till shortly. The next paper, of Ken Poulton, addresses the Bipolar/CMOS trends and the shift in the last five years to CMOS. The pipelined converter slices of the time-interleaved architecture are made in full-CMOS; a separate SiGe chip comprises the only function left for bipolar in this design: the buffering.

As suggested earlier, time-interleaved flash and time-interleaved pipelines are not the only architectures that are considered nowadays. Other architectures like successive approximation converters (SAR), subranging converters, time-inteleaved folding converters, and sub-harmonic limit-cycle sigma-delta (SLC-SDM) conversion will be addressed too, in the next papers.

Dieter Draxelmayr, in his paper, demonstrates similarities and differences between pipelined, algorithmic, and SAR converters. He addresses the various algorithmic and circuit level adaptations that can improve speed, and the calibration methods that can improve the accuracy while alleviating the requirements on the building blocks and technology.

The next paper, from Frank van der Goes, presents again a different architecture: the two-step subranging ADC. He addresses the design of a family of converters ranging from 8 bit to 10 bit at sampling rates from 50MS/s up to 200MS/s.
Robert Taft focuses on various ways of offset calibration and applies it to a 2x interleaving 8bit folding interpolating flash ADC operating at 1.6GS/s, where he solves the offset problem with a one-time foreground calibration.

Finally, we have a paper on the sigma-delta type of converters. These converters have several beneficial properties, but the main drawback is the limited bandwidth due to the required oversampling ratio. In this paper it is shown that also this speed boundary can be shifted, by a better understanding and modeling of the non-linear loop, especially by understanding the limit cycles. By using a new mode of operation, Subharmonic Limit-Cycle SDMs are obtained that achieve significantly improved performance.

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