CMOS Cascade Sigma-Delta Modulators for Sensors and Telecom
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Error Analysis and Practical Design

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<tr>
<td>ΠΣΔ</td>
<td>Parallel Sigma-Delta</td>
</tr>
<tr>
<td>ΣΔ</td>
<td>Sigma-Delta</td>
</tr>
<tr>
<td>ΣΔM</td>
<td>Sigma-Delta Modulator</td>
</tr>
<tr>
<td>A/D, A-to-D</td>
<td>Analog-to-Digital</td>
</tr>
<tr>
<td>ADC</td>
<td>Analog-to-Digital Converter</td>
</tr>
<tr>
<td>ADSL</td>
<td>Asymmetric Digital Subscriber Line</td>
</tr>
<tr>
<td>AFE</td>
<td>Analog Front-End</td>
</tr>
<tr>
<td>AGC</td>
<td>Automatic Gain Control</td>
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<tr>
<td>BiCMOS</td>
<td>Bipolar and Complementary Metal-Oxide-Semiconductor</td>
</tr>
<tr>
<td>BΡΣΔM</td>
<td>Band-Pass Sigma-Delta Modulator</td>
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<tr>
<td>CAD</td>
<td>Computer Aided Design</td>
</tr>
<tr>
<td>CDMA</td>
<td>Code Division Multiple Access</td>
</tr>
<tr>
<td>CLA</td>
<td>Clocked Averaging</td>
</tr>
<tr>
<td>CMFB</td>
<td>Common-Mode Feedback</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary Metal-Oxide-Semiconductor</td>
</tr>
<tr>
<td>CPE</td>
<td>Customer Premises Equipment</td>
</tr>
<tr>
<td>CPU</td>
<td>Central Processing Unit</td>
</tr>
<tr>
<td>CT</td>
<td>Continuous-Time</td>
</tr>
<tr>
<td>D/A, D-to-A</td>
<td>Digital-to-Analog</td>
</tr>
<tr>
<td>DAC</td>
<td>Digital-to-Analog Converter</td>
</tr>
<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>DDS</td>
<td>Data Directed Scrambling</td>
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<tr>
<td>DEM</td>
<td>Dynamic Element Matching</td>
</tr>
<tr>
<td>DMT</td>
<td>Discrete Multi-Tone</td>
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<tr>
<td>DNL</td>
<td>Differential Non-Linearity</td>
</tr>
<tr>
<td>DOR</td>
<td>Digital Output Rate</td>
</tr>
<tr>
<td>DR</td>
<td>Dynamic Range</td>
</tr>
<tr>
<td>DSL</td>
<td>Digital Subscriber Line</td>
</tr>
<tr>
<td>DSP</td>
<td>Digital Signal Processing</td>
</tr>
<tr>
<td>DT</td>
<td>Discrete-Time</td>
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<tr>
<td>DWA</td>
<td>Data Weighted Averaging</td>
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<tr>
<td>EDGE</td>
<td>Enhanced Data-rates for Global Evolution</td>
</tr>
<tr>
<td>ENOB</td>
<td>Effective Number Of Bits</td>
</tr>
<tr>
<td>ESD</td>
<td>Electrostatic Discharge</td>
</tr>
<tr>
<td>Abbreviation</td>
<td>Description</td>
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<tr>
<td>--------------</td>
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<tr>
<td>FFT</td>
<td>Fast Fourier Transform</td>
</tr>
<tr>
<td>FIR</td>
<td>Finite Impulse Response</td>
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<tr>
<td>FOM</td>
<td>Figure Of Merit</td>
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<tr>
<td>FS</td>
<td>Full Scale</td>
</tr>
<tr>
<td>GB</td>
<td>Gain-Bandwidth Product</td>
</tr>
<tr>
<td>GPS</td>
<td>Global Positioning System</td>
</tr>
<tr>
<td>GSM</td>
<td>Global System for Mobile-Communications</td>
</tr>
<tr>
<td>HD</td>
<td>Harmonic Distortion</td>
</tr>
<tr>
<td>HDSL</td>
<td>High-data-rate Digital Subscriber Line</td>
</tr>
<tr>
<td>IBE</td>
<td>In-Band Error</td>
</tr>
<tr>
<td>IC</td>
<td>Integrated Circuit</td>
</tr>
<tr>
<td>IIR</td>
<td>Infinite Impulse Response</td>
</tr>
<tr>
<td>ILA</td>
<td>Individual Level Averaging</td>
</tr>
<tr>
<td>INL</td>
<td>Integral Non-Linearity</td>
</tr>
<tr>
<td>IO</td>
<td>Input/Output</td>
</tr>
<tr>
<td>ISDN</td>
<td>Integrated Services Digital Network</td>
</tr>
<tr>
<td>LNA</td>
<td>Low-Noise Amplifier</td>
</tr>
<tr>
<td>LPΣΔM</td>
<td>Low-Pass Sigma-Delta Modulator</td>
</tr>
<tr>
<td>LSB</td>
<td>Least Significant Bit</td>
</tr>
<tr>
<td>MASH</td>
<td>Multi-Stage Noise Shaping</td>
</tr>
<tr>
<td>MEMS</td>
<td>Micro-Electro-Mechanical System</td>
</tr>
<tr>
<td>MiM</td>
<td>Metal-insulator-Metal</td>
</tr>
<tr>
<td>MOS</td>
<td>Metal-Oxide-Semiconductor</td>
</tr>
<tr>
<td>MOSFET, MOST</td>
<td>Metal-Oxide-Semiconductor Field-Effect Transistor</td>
</tr>
<tr>
<td>MSB</td>
<td>Most Significant Bit</td>
</tr>
<tr>
<td>MTPR</td>
<td>Multi-Tone Power Ratio</td>
</tr>
<tr>
<td>nMOS</td>
<td>N-channel MOS</td>
</tr>
<tr>
<td>NTF</td>
<td>Noise Transfer Function</td>
</tr>
<tr>
<td>Opamp</td>
<td>Operational Amplifier</td>
</tr>
<tr>
<td>OS</td>
<td>Output Swing</td>
</tr>
<tr>
<td>OSR</td>
<td>Oversampling Ratio</td>
</tr>
<tr>
<td>OTA</td>
<td>Operational Transconductance Amplifier</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed Circuit Board</td>
</tr>
<tr>
<td>PDF</td>
<td>Probability Density Function</td>
</tr>
<tr>
<td>PDM</td>
<td>Pulse-Density Modulated</td>
</tr>
<tr>
<td>PLC</td>
<td>Power Line Communications</td>
</tr>
<tr>
<td>Abbreviation</td>
<td>Description</td>
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<td>--------------</td>
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</tr>
<tr>
<td>PLL</td>
<td>Phase-Locked Loop</td>
</tr>
<tr>
<td>pMOS</td>
<td>P-channel MOS</td>
</tr>
<tr>
<td>PROM</td>
<td>Programmable Read-Only Memory</td>
</tr>
<tr>
<td>PSD</td>
<td>Power Spectral Density</td>
</tr>
<tr>
<td>RAM</td>
<td>Random Access Memory</td>
</tr>
<tr>
<td>RF</td>
<td>Radio Frequency</td>
</tr>
<tr>
<td>ROM</td>
<td>Read-Only Memory</td>
</tr>
<tr>
<td>S/H</td>
<td>Sample-and-Hold</td>
</tr>
<tr>
<td>SC</td>
<td>Switched-Capacitor</td>
</tr>
<tr>
<td>SDLS</td>
<td>Symmetrical Digital Subscriber Line</td>
</tr>
<tr>
<td>SFDR</td>
<td>Spurious-Free Dynamic Range</td>
</tr>
<tr>
<td>SI</td>
<td>Switched-Current</td>
</tr>
<tr>
<td>SNR</td>
<td>Signal-to-Noise Ratio</td>
</tr>
<tr>
<td>SNDR</td>
<td>Signal-to-(Noise+Distortion) Ratio</td>
</tr>
<tr>
<td>SoC</td>
<td>System-on-Chip</td>
</tr>
<tr>
<td>SR</td>
<td>Slew Rate</td>
</tr>
<tr>
<td>STF</td>
<td>Signal Transfer Function</td>
</tr>
<tr>
<td>THD</td>
<td>Total Harmonic Distortion</td>
</tr>
<tr>
<td>TΣΔ</td>
<td>Time-Interleaved Sigma-Delta</td>
</tr>
<tr>
<td>UMTS</td>
<td>Universal Mobile Telecommunications System</td>
</tr>
<tr>
<td>UWB</td>
<td>Ultra-Wide Band</td>
</tr>
<tr>
<td>VDSL</td>
<td>Very-high-data-rate Digital Subscriber Line</td>
</tr>
<tr>
<td>VLSI</td>
<td>Very Large Scale of Integration</td>
</tr>
<tr>
<td>WLAN</td>
<td>Wireless Local Area Network</td>
</tr>
<tr>
<td>WMAN</td>
<td>Wireless Metropolitan Area Network</td>
</tr>
<tr>
<td>xDSL</td>
<td>All/any Digital Subscriber Line</td>
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</tbody>
</table>
The rapid evolution experimented by microelectronics during the last decades has propitiated the birth and spread of lots of electronic systems with increasing presence in different aspects of our everyday life: consumer electronics, information technology, communications, automation, medicine, leisure, etc. Probably, communications has been one of the areas with largest expansion; many applications have been developed, both for wireline systems—DSL technologies for broadband access to the Internet, PLC technology, etc. [Gagn97]—and for wireless systems—mobile telephony, GPS, WLAN, WMAN, UWB, etc. [Abidi95].

No doubt, the continuous scaling of VLSI technologies has been a determinant factor for this rapid evolution. Technology scaling has allowed miniaturization, portability, increased functionality, and cost reduction of these systems. Nowadays, it is possible to integrate millions of transistors in a single chip using submicron CMOS processes and, simultaneously, the speed of digital circuits has increased up to the gigahertz range. This technological advances have enabled monolithic integration of complete electronic systems on a single chip (SoC), in which digital signal processing (DSP) techniques are extensively used for robust implementation of complex algorithms within reduced computational times.

In these systems, the present trend is to move the border between the analog and digital parts, usually called interface, as close as possible to the point where information is received or emitted. In this way, most of the SoC functionalities are implemented in the digital domain, where the system benefits from the reduction of silicon area, supply voltage, and power consumption, and from the increased operation speed that are peculiar to the progressive technology scaling. The application of analog circuits is then restricted, in most cases, to interface tasks: signal conditioning, filtering, and analog-to-digital (A-to-D) and digital-to-analog (D-to-A) conversion. In addition, the trend to massive digital processing and to an earlier digitalization of signals leads to an increase of the dynamic range and bandwidth requirements in the interface circuits.

On the other hand, the design of high resolution, high bandwidth converters is greatly involved when they are integrated together with the DSP circuits, mainly because the designers must use mainstream digital CMOS processes, in which analog primitives are not fully optimized [Bult00] [Malo01]. Thus, these converters have to operate with low voltage supply and transistors whose threshold voltages are comparatively high, with no use of extra process steps to improve the linearity or the matching of the devices, and, above all, in an hostile environment full of noisy digital circuits.

Among the existing techniques to perform the A-to-D conversion, those based on $\Sigma\Delta$ modulation [Inose62] offer key advantages for their implementation in SoCs. Unlike traditional converters, which require high accuracy in their building blocks in order to
achieve overall high accuracy, the oversampling and noise-shaping techniques employed in \( \Sigma \Delta \) converters allow to trade speed for accuracy. In this way, an operation that is relatively insensitive to imperfections on the analog circuit can be obtained at the cost of increased complexity and speed in the associated digital circuitry (needed for post-processing) [Nors97].

These demanding requirements on the digital part, which were a handicap for the integration of \( \Sigma \Delta \) converters before the development of VLSI technologies, now relax the implementation of the analog section, whose requirements are more difficult to achieve in processes with a clear digital orientation. This has motivated that, although being originally conceived for low-frequency, high-resolution applications like audio [Candy85] [Adams86] [Boser88] [Bran91a] and precision measurement [Sign90] [Yama94], the usage of \( \Sigma \Delta \) converters has progressively spreaded across medium- and high-frequency applications [Bran91b] [OptE91] [Yin94] [Broo97].

Fig. 1 illustrates the state of the art in A-to-D converters in CMOS technologies reported up to year 2000 and places them in the resolution—bandwidth plane. The ranges of the specifications for the main applications are depicted on this plane in an approximated way. It can be observed that \( \Sigma \Delta \) modulation-based A-to-D converters cover a wide frequency

![FIGURE 1](image-url)  
State of the art in A-to-D converters in CMOS technologies reported up to year 2000. (The ranges of the applications shown are approximated).
interval, ranging from 100Hz to 10MHz. Higher speed applications are still dominated by Nyquist-type converters (especially, pipeline, folding-interpolative, and flash) [Plas94] [Raza95]. Oversampling techniques are little efficient in these applications, because of the excessive operation speed that is required in the analog blocks. However, $\Sigma\Delta$ converters are clearly dominant in measurement, voice, and audio systems, and coexist with algorithmic, subranging, and pipeline converters in systems for mobile communications and broadband wireline applications like ADSL. Furthermore, it is commonly accepted that whenever an industrial application can be covered by using a $\Sigma\Delta$ converter, the simpler the better, this solution should be considered as the optimum one, for feasibility, yield, robustness, and time-to-market reasons [Rivo03].

In these applications, the implementation of Nyquist converters gets involved as the technology scales down: calibration techniques that consume considerable area and power are required in order to achieve resolutions larger than 13 bits [Mayes96] [Opris00] [Guil01]. As an alternative, the use of $\Sigma\Delta$ converters has gained ground and architectures that are oriented to high-frequency applications have been successfully implemented. In these architectures, the weakened benefits of oversampling (necessarily moderate) are compensated by resorting to high-order topologies—either in a single loop [Geer00] or in a multi-stage cascade [Yin94] [Feld98] [Marq98] [Geer99] [Mori00]—, which often incorporate multi-bit quantization—either pure [Geer00] [Fuji00] or by means of dual-quantization techniques [Bran91b] [Broo97] [Mede99].

Nevertheless, the prototypes implemented so far demonstrate the viability of $\Sigma\Delta$ converters for high-frequency applications (>1MHz), but not that their incorporation to SoCs is still robust in deep-submicron processes. Indeed, only a few prototypes [Geer99] [Fuji00] [Mori00] have been integrated in modern deep-submicron CMOS technologies, but they are mixed-signal oriented—they offer better device matching and supply voltages of 3.3V, or even 5V, together with low-Vt transistors [Fuji00].

In this scenario, the work presented in this book tries to demonstrate the viability of robust high-frequency, high-resolution $\Sigma\Delta$ converters using deep-submicron CMOS technologies oriented to the development of SoCs. This encompasses an adequate selection of architectures, techniques, and building blocks that allow, not only to obtain high-performance $\Sigma\Delta$ modulators, but also to solve the problems associated to their practical implementation in digital-oriented VLSI technologies (low supply voltage, poor linearity and matching of devices, etc.).

The results of this work are demonstrated through two prototypes for broadband applications that are integrated in deep-submicron CMOS technologies. They have been developed in the frame of the EU ESPRIT Project 29261 (MIXMODEST) and the Spanish CICYT Projects TIC97-05080 and TIC2001-0929 (ADAVERE), devoted to the investigation of architectures and techniques for the implementation of A-to-D converters in last generation CMOS technologies.
The first prototype is a wideband 2-1-1 ΣΔ cascade with dual quantization of 1 and 4 bits, which has been implemented in a 0.35-μm standard digital CMOS process with epitaxial (low-ohmic, conductive) substrate. The modulator operates with an oversampling ratio of 16 and exhibits a differential full-scale range of 4V using the 3.3-V nominal supply voltage. It achieves an effective resolution of 13bit at 4MS/s and consumes 78mW, while operated at 64-MHz internal clock frequency.

The second design is conceived to be incorporated to a CPE modem for ADSL and ADSL+ in a 2.5-V 0.25-μm CMOS process. The selected topology is a 2-1-1 cascade with quantization of 1 and 3 bits, which operates with an oversampling ratio of 32 or 16, and exhibits a differential full-scale range of 3V. The prototype achieves an effective resolution of 13.8bit at 2.2MS/s and 12.7bit at 4.4MS/s, with a power consumption of 66mW, while operating with a sampling frequency of 70.4MHz.

The book also presents the design of a third prototype to be included in an automotive sensor interface in a 3.3-V 0.35-μm CMOS process. The modulator topology is a 2-1 single-bit ΣΔ cascade that can be digitally programmed to yield four gain values—× 0.5, × 1, × 2, and × 4—in order to obtain a better fitting to the different sensor outputs. This prototype has been developed in the frame of the EU ESPRIT Project 34283 (TAMES-2), whose objective is to improve the industrial testability of high-resolution A-to-D interfaces embedded in SoCs. The modulator achieves an effective resolution of 18bit at 40kS/s and consumes 14.7mW, while operated at 5.12-MHz internal clock frequency.

The three prototypes presented in the book avoid the use of calibration techniques, non-standard transistors, or on-chip voltages larger than the nominal supply, and their performances are competitive to the current state of the art.

The contents of the book are organized in five chapters.

Chapter 1 presents an introduction to ΣΔ A-to-D converters, showing the principles of operation, the basic architectures, and the ideal performance of ΣΔ modulators. Topologies for their practical implementation are introduced and their pros and cons are discussed. The state of the art in low-pass ΣΔ modulators in CMOS technologies is then revised, showing existing trends in present designs.

Chapter 2 is dedicated to the exhaustive analysis of the main non-idealities that affect the performance of ΣΔ modulators. System considerations, behavioral models, and closed expressions are obtained for the impact of the different non-idealities, which can be used as estimable guidelines for practical implementation of ΣΔ modulators.

Chapters 3 and 4 describe the design of the two ΣΔ modulators intended for broadband applications, whereas Chapter 5 describes the design of the ΣΔ modulator with programmable gain for automotive sensor interfaces. The topology selection, the requirements of the building blocks, and their design at the transistor level are deeply
discussed. The measured performance for the prototypes is presented and compared with the state-of-the-art ΣΔ modulators.

The considerations presented through the book for the design of cascade ΣΔ modulators in deep-submicron CMOS are extended in Appendixes A and B. Appendix A proposes a family of cascade ΣΔ modulators that is easily expandible to high order, while preserving a low systematic loss of resolution and a high overload level. An analytical method to estimate its power consumption is presented in Appendix B.
References to the Preface


