Part VI focuses on advanced multilevel interconnects, contributed by distinguished authors in the following sections: “Introduction to Electrochemical Process Integration for Cu Interconnects” (Chapter 17), “Damascene Concept and Process Steps” (Chapter 18), “Advanced BEOL Technology Overview” (Chapter 19), “Lithography for Cu Damascene Fabrication” (Chapter 20), “Physical Vapor Deposition Barriers for Cu Metallization PVD Barriers” (Chapter 21), “Low-K dielectrics” (Chapter 22), “CMP for Cu Processing” (Chapter 23), “Electrochemical View of Copper Chemical Mechanical Polishing” (CMP) (Chapter 24), “Copper Post-CMP Cleaning” (Chapter 25). Chapter 17 gives brief introduction to electrochemical process integration for Cu interconnects. Chapter 18 describes about the damascene process for Cu interconnect formation. There are two damascene processes: single and dual. Using Cu as an alternative for Al was a drastic change for reducing the interconnect resistance. Technological challenges are being faced in the development of low dielectric-constant ($k$) dielectrics for reducing the parasitic capacitance of Cu interconnects given in a separate section. This chapter also describes the need of damage-free damascene process. Chapter 19 presents the overview for the BEOL technology for 90 nm and 65 nm/45 nm node and presents the low-$k$ material for each technology node and metallization issues. This part also presents the process development tools for establishing the robust process and the characterization development for patterned low-$k$ films. Both items will be necessary for future BEOL process development. Chapter 20 deals with the lithography for copper damascene fabrication. For the DD interconnect fabrication, interconnect trench and via holes are patterned in the ILD film sequentially. The multi-hard-mask (MHM) processes are innovated to avoid the oxygen plasma damage observed in the conventional photo-resist (PR) mask process, however, the line top spreading (LTS) and the line edge roughness (LER) are the main issues. The lithography sequence such as the via-first or the trench-first processes affects the misalignment margin between the lines and vias. We should design the lithography process sequence carefully by taking the material combination and the misalignment margin into considerations. Chapter 21 describes the necessity of diffusion barrier layer and gives the thermophysical characteristics which play significant role in the selection of metallurgy for barrier material selection. It also includes the barrier formation technique and its kinetics. Chapter 22 gives the details about low-$k$ dielectrics such as basic properties and innovations of
low-\(k\) material and process. Introduction of low-\(k\) dielectric film, especially porous film, is a key factor to reduce the parasitic capacitance (\(C_{\text{int}}\)) among multi-layer interconnects in leading-edge ULSI devices. The mechanical properties as well as the electrical reliability depend on the physical and chemical structure in the porous film. New innovations have been implemented such as EB/UV post-curing process and molecule structural design to stabilize the porous films. Reduction in the \(k\)-values of barrier dielectrics or capping films becomes important to decrease \(C_{\text{int}}\) effectively especially for 45/32 nm nodes. Chapter 23 presents the CMP review for Cu processing and includes general principals for Cu CMP and planarization. CMP (chemical mechanical polisher) is now regarded as an essential process among semiconductor device manufacturing processes. This CMP was first introduced by IBM in early 1980s for planarization of logic devices. Chemical mechanical polishing or planarization (CMP) aims at the removal of overburden copper after its electrochemical deposition. CMP primer objective is to achieve a global planarization of patterned surface. CMP appears to be the most promising pattern delineation technique. Chapter 24 gives electrochemical view of copper chemical mechanical polishing (CMP) in detail using different solutions such as ammonium hydroxide, nitric acid, peroxide and carbonate and sorbate-based solutions along with respective polarization curves. Chapter 25 describes copper post-CMP cleaning process as it is an important step in damascene technology utilizing copper on-chip interconnects. This process can significantly improve wafer surface quality by removing different defects and contaminations from copper layers and ILD. Etching of wafer surface plays an important role in abrasive particles’ removal from the copper surface layer and interlayer dielectric. Copper layers are mostly contaminated with abrasive particles which determine strategy and procedure of post-CMP cleaning. HNO\(_3\)-based solutions are highly effective in copper layers etching. Simultaneous etching of silicon oxide and copper layers can be efficiently conducted in diluted HF solutions. However, copper etching in aqueous solutions is usually accompanied with a deposition of corrosion products (Cu(1) compounds). Formation of such deposition is being determined electrochemically subsequent to an etching process (at OCP) in some of the recommended post-CMP cleaning solutions. These results imply that one should be very cautious in choosing the most appropriate etching solution for Cu post-CMP cleaning.