Part II
Technology Background

Part II presents the technological background for interconnect in ULSI systems. It includes detailed description of MOS device and interconnects scaling physics (Chapter 2). Chapter 3 is about electrical performance of Cu interconnects for ULSI applications. It is well known that the steady growth in complexity of integrated electronic systems requires a growing number of metal interconnect layers in ULSI chips. The role of interconnects in integrated electronic systems is described in this chapter: Metrics for evaluating the quality of signal interconnections are presented, and simple electrical circuit models for interconnects are introduced. In light of these models, the fundamental problem of interconnect scaling is presented and design approaches for addressing the problem are briefly surveyed. As there are lots of deposition techniques, either electroless or electrodeposition, available elsewhere Chapter 4 presented a brief description of electrodeposition process and a focused discussion of copper electrodeposition for chip interconnects. It must be emphasized that different chip manufacturers have their unique combination of electrodeposition tools, proprietary tailored bath, and integration scheme for copper chip interconnects. Successful implementation of the copper electrodeposition process in high-volume chip manufacturing involves equal attention to metrology, process integration, and reliability issues. Besides void-free deposition of interconnect structures, selection of a reliable CMP process, excellent adherence of copper lines/vias to the dielectric, low resistivity, and resistance to electromigration are some of the key requirements for a high-yielding, reliable interconnect electrodeposition process. All these aspects are addressed in greater detail in different chapters of this book. Along with this Chapter 5, “Electrophoretic Deposition,” defined the process of electrophoretic deposition and the process is summarized. The limitations of the process are explained and potential applications in the microelectronics sector are identified. Three areas in which industrial feasibility has been explored are then described in more detail. In addition to deposition technologies, proper device integration technology is important. As wafer-level 3D integration (i.e., 3D stacking prior to singulation of wafers into individual chips) has become an increasingly active research topic, without any large-scale IC manufacturing, Chapter 6 “Wafer Level 3D Integration for ULSI Interconnects” presents types of 3D integration, BEOL-based wafer-level 3D processing and wafer-level 3D design opportunities. Wafer-level interconnectivity is extended to multiple device levels.