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Leakage in Nanometer CMOS Technologies
Siva G. Narendra and Ananth Chandrakasan
LEAKAGE IN NANOMETER CMOS TECHNOLOGIES

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## Contents

**Preface** ix

1. **Taxonomy of Leakage: Sources, Impact, and Solutions**
   1.1 Introduction 1
   1.2 Sources 3
   1.3 Impact 11
   1.4 Solutions 13
   References 18

2. **Leakage Dependence on Input Vector**
   SIVA NARENDRA, YIBIN YE, SHEKAR BORKAR, VIVEK DE, AND ANANTHA CHANDRAKASAN
   2.1 Introduction 21
   2.2 Stack Effect 23
   2.3 Leakage Reduction using Natural Stacks 30
   2.4 Leakage Reduction using Forced Stacks 35
   2.5 Summary 38
   References 39

3. **Power Gating and Dynamic Voltage Scaling**
   BENTON CALHOUN, JAMES KAO, AND ANANTHA CHANDRAKASAN
   3.1 Introduction 41
   3.2 Power Gating 41
### 4. Methodologies for Power Gating
KIMIYOSHI USAMI AND TAKAYASU SAKURAI

<table>
<thead>
<tr>
<th>Section</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.1</td>
<td>Introduction</td>
<td>77</td>
</tr>
<tr>
<td>4.2</td>
<td>Power Gating Methodologies for Real Designs</td>
<td>79</td>
</tr>
<tr>
<td>4.3</td>
<td>Future Directions of Power Gating</td>
<td>90</td>
</tr>
<tr>
<td>4.4</td>
<td>Summary</td>
<td>102</td>
</tr>
<tr>
<td></td>
<td>References</td>
<td>103</td>
</tr>
</tbody>
</table>

### 5. Body Biasing
TADAHIRO KURODA AND TAKAYASU SAKURAI

<table>
<thead>
<tr>
<th>Section</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>5.1</td>
<td>Introduction</td>
<td>105</td>
</tr>
<tr>
<td>5.2</td>
<td>Reverse Body Bias</td>
<td>107</td>
</tr>
<tr>
<td>5.3</td>
<td>Forward Body Bias</td>
<td>126</td>
</tr>
<tr>
<td>5.4</td>
<td>Future Directions</td>
<td>137</td>
</tr>
<tr>
<td></td>
<td>References</td>
<td>139</td>
</tr>
</tbody>
</table>

### 6. Process Variation and Adaptive Design
SIVA NARENDRA, JAMES TSCHANZ, JAMES KAO, SHEKAR BORKAR, ANANTHA CHANDRAKASAN, AND VIVEK DE

<table>
<thead>
<tr>
<th>Section</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>6.1</td>
<td>Introduction</td>
<td>141</td>
</tr>
<tr>
<td>6.2</td>
<td>Bi-directional Adaptive Body Bias</td>
<td>143</td>
</tr>
<tr>
<td>6.3</td>
<td>Body Bias Circuit Impedance</td>
<td>150</td>
</tr>
<tr>
<td>6.4</td>
<td>Adaptive Supply Voltage and Adaptive Body Bias</td>
<td>156</td>
</tr>
<tr>
<td></td>
<td>References</td>
<td>162</td>
</tr>
</tbody>
</table>

### 7. Memory Leakage Reduction
TAKAYUKI KAWAHARA AND KIYOO ITOH

<table>
<thead>
<tr>
<th>Section</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>7.1</td>
<td>Introduction</td>
<td>163</td>
</tr>
<tr>
<td>7.2</td>
<td>Leakage in RAMs</td>
<td>164</td>
</tr>
<tr>
<td>7.3</td>
<td>Leakage Sources and Reduction in RAMs</td>
<td>168</td>
</tr>
<tr>
<td>7.4</td>
<td>Various Leakage Reduction Schemes</td>
<td>171</td>
</tr>
<tr>
<td>7.5</td>
<td>Gate-Source Reverse Biasing Schemes</td>
<td>175</td>
</tr>
<tr>
<td>7.6</td>
<td>Applications to RAM Cells</td>
<td>180</td>
</tr>
<tr>
<td>7.7</td>
<td>Applications to Peripheral Circuits</td>
<td>186</td>
</tr>
<tr>
<td>7.8</td>
<td>Future Prospects</td>
<td>195</td>
</tr>
<tr>
<td>7.9</td>
<td>Conclusion</td>
<td>196</td>
</tr>
<tr>
<td></td>
<td>References</td>
<td>196</td>
</tr>
</tbody>
</table>
8. Active Leakage Reduction and Multi-Performance Devices

SIVA NARENDRA, JAMES TSCHANZ, SHEKAR BORKAR, AND VIVEK DE

8.1 Introduction 201
8.2 Standby Techniques for Active Leakage Reduction 202
8.3 Multi-performance Devices 208
References 209

9. Impact of Leakage Power and Variation on Testing

ALI KESHAVARZI AND KAUSHIK ROY

9.1 Introduction 211
9.2 Background 212
9.3 Leakage vs. Frequency Characterization 214
9.4 Multiple-Parameter Testing 216
9.5 Sensitivity Gain with RBB and Temperature 218
9.6 Leakage versus Temperature Two-Parameter Test Solution 227
9.7 Discussions and Test Applications 229
9.8 Conclusion 232
References 232

10. Case Study: Leakage Reduction in Hitachi/Renesas Microprocessors

MASAYUKI MIYAZAKI, HIROYUKI MIZUNO, AND TAKAYUKI KAWAHARA

10.1 Leakage Reduction Using Body Bias in a RISC Microprocessor 235
10.2 Leakage Reduction in Application Processor in 3G Cellular Phone 240
10.3 Leakage Reduction in SRAM module 249
References 255

11. Case Study: Leakage Reduction in the Intel Xscale Microprocessor

LAWRENCE CLARK

11.1 Introduction 257
11.2 Circuit Configuration and Operation 261
11.3 Regulator Design 267
11.4 Time-Division Multiplexed Operation 273
11.5 SOC Design Issues and Future Trends 276
11.6 Conclusion 278
12. Transistor Design to Reduce Leakage

SAGAR SUTHRAM, SIVA NARENDRA, AND SCOTT THOMPSON

12.1 Introduction
12.2 Sub-threshold Leakage in Nanoscale Planar Si MOSFETs
12.3 SiON Dielectrics to Reduce Gate to Channel Direct Tunneling Current
12.4 Offset Spacers to Reduce Edge Direct Tunneling Current
12.5 Compensation Implants to Reduce Junction Leakage
12.6 Source/Drain Extension Grading to Reduce Gate Induced Drain Leakage (GIDL)
12.7 Future Solutions
12.8 Summary
References

Index
Preface

Scaling transistors into the nanometer regime has resulted in a dramatic increase in MOS leakage (i.e., off-state) current. Threshold voltages of transistors have scaled to maintain performance at reduced power supply voltages. Leakage current has become a major portion of the total power consumption, and in many scaled technologies leakage contributes 30-50% of the overall power consumption under nominal operating conditions. Leakage is important in a variety of different contexts. For example, in desktop applications, active leakage power (i.e., leakage power when the processor is computing) is becoming significant compared to switching power. In battery operated systems, standby leakage (i.e., leakage when the processor clock is turned off) dominates as energy is drawn over long idle periods.

Increased transistor leakages not only impact the overall power consumed by a CMOS system, but also reduce the margins available for design due to the strong relationship between process variation and leakage power. It is essential for circuit and system designers to understand the components of leakage, sensitivity of leakage to different design parameters, and leakage mitigation techniques in nanometer technologies. This book provides an in-depth treatment of these issues for researchers and product designers.

This book also provides an understanding of various leakage power sources in nanometer scale MOS transistors. Leakage sources at the MOS transistor level including sub-threshold, gate tunneling, and junction currents will be discussed. Manifestation of these MOS transistor leakage components at the full chip level depends considerably on several aspects including the nature of the circuit block, its state, its application workload, and process/voltage/temperature conditions. The sensitivity of the various MOS
leakage current sources at the transistor level to these conditions will be introduced. These leakage currents at the transistor level translate to the system level in various ways and therefore impact the overall system in a diverse manner. For example, transistor leakages manifest differently under normal operation compared to typical testing conditions, such as burn-in testing. Transistor leakages impact power consumption of the system depending on the system state (e.g., active condition vs. standby condition). Active system leakage power can be significantly higher than standby system leakage, due to elevated temperature and the difficulty to trade-off leakage power for performance. The impact of leakage components also depends on the style of circuit and module type (e.g., memory vs. logic).

To deal with transistor leakage, a variety of solutions is required at all levels of design. The solutions include leakage modeling and prediction, transistor modifications, circuit techniques and system modifications. This book provides an in-depth coverage of promising techniques at the transistor, circuit, and architecture levels of abstraction.

The topics discussed in this book include sources of transistor leakage and its impact, state assignment based leakage reduction, power gating techniques, dynamic voltage scaling, body-biasing, use of multiple performance transistors, leakage reduction in memory, impact of process variation on leakage and design margins, active leakage power reduction techniques, and impact of process variation and leakage on testing. Additionally, two case studies will be presented to highlight real world examples that reap the benefits of leakage power reduction solutions. The last chapter of the book will highlight transistor design choices to mitigate the increase in the leakage components as technology continues to scale.

This book would not have been possible without the concerted effort of all its contributing authors. We would like to thank them for their contribution and help with reviewing other chapters to ensure consistency. We would also like to express sincere thanks to non-contributing reviewers—Dinesh Somashekar and Keith Bowman, both of Intel Corporation. I (Siva) would like to recognize the dedicated contribution of my late colleague and friend at Intel Corporation, Brad Bloechel, without whom, lot of the experimental results in the chapters 2, 6, 8, and 9 would not have been possible. He will be missed. Finally, we want to thank our families for their patience and support through the process of compiling this book together.

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