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Zhiqiang Li

The Source/Drain Engineering of Nanoscale Germanium-based MOS Devices

Doctoral Thesis accepted by
Peking University, Beijing, China

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[1] **Zhiqiang Li**, Xia An, Min Li, Quanxin Yun, Meng Lin, Ming Li, Xing Zhang, and Ru Huang, "Low Electron Schottky Barrier Height of NiGe/Ge Achieved by Ion-Implantation after Germanidation Technique," ***IEEE Electron Device Lett.,*** vol. 33, no. 12, pp. 1687–1689, Dec. 2012.

[2] **Zhiqiang Li**, Xia An, Min Li, Quanxin Yun, Meng Lin, Ming Li, Xing Zhang, and Ru Huang, "Morphology and Electrical Performance Improvement of NiGe/Ge Contact by P and Sb Co-implantation," ***IEEE Electron Device Lett.,*** vol. 34, no. 5, pp. 596–598, May. 2013.

[3] **Zhiqiang Li**, Xia An, Quanxin Yun, Meng Lin, Min Li, Ming Li, Xing Zhang, and Ru Huang, "Low Specific Contact Resistivity to n-Ge and Well-Behaved Ge n^+/p Diode Achieved by Multiple Implantation and Multiple Annealing Technique," ***IEEE Electron Device Lett.,*** vol. 34, no. 9, pp. 1097–1099, Sep. 2013.

[4] **Zhiqiang Li**, Xia An, Min Li, Quanxin Yun, Meng Lin, Ming Li, Xing Zhang, and Ru Huang, "Study on Schottky Barrier Modulation of NiGe/Ge by Ion-implantation after Germanidation Technique," ***The 11th ICSICT,*** Xi'an, 2012.

Supervisors' Foreword

With continuous development of integrate circuit in the past 40 years, transistor scaling has been the driving force for technology advancement in the semiconductor industry. However, performance gain becomes more and more difficult as device dimension shrinks into the nanoscale regime, and material innovation is one of the primary enablers for further performance enhancement of CMOS technology. Recently, Ge has attracted much attention owing to its high and symmetric mobilities of electron and hole. Although much improvement has been achieved in Ge-based device, several principal issues still need to be solved for realizing high performance Ge MOSFETs, including the source/drain (S/D) engineering in Ge nMOSFETs.

It is well recognized that one of the critical challenges of nanoscale MOSFET is reducing the impact of parasitic source/drain series resistance, which is more serious in the source/drain of Ge nMOS device, due to the severe Fermi level pinning effect, poor thermal stability of NiGe, and low n-type dopant activation concentration in Ge. Therefore, this Ph.D. thesis by Dr. Zhiqiang Li has focused on the source/drain engineering of Ge nMOSFETs, aiming to reduce the source/drain parasitic resistance. Dr. Li has broad vision and is skilled at identifying the main or controlling factor in daedal situations, and thus significant progress has been made in these fields.

The obvious scientific achievements achieved in this thesis can be divided into several parts. First, implantation after germanide (IAG) technique is applied to modulate the electron SBH of metal/n-Ge contact, and extremely low electron SBH of 0.1 eV is achieved with optimized process parameters. Second, P and Sb co-implantation technique is adopted to improve the thermal stability of NiGe. Both the morphology and electrical performance of NiGe/Ge contact is greatly improved by this technique, and its thermal stability is enhanced at least to 600 °C. Finally, multiple implantation and multiple annealing technique is proposed to reduce the contact resistivity of metal contact to n-Ge, where high electrical activation over 1×10^{20} cm^{-3} and low specific contact resistivity of 3.8×10^{-7} Ω cm^2 is obtained.

These achievements are beneficial for the performance improvement of Ge nMOSFETs.

This thesis has provided effective methods for the aforementioned issues associated with source/drain design of Ge nMOSFETs. Both experiment data and theoretical analysis are accurate and reliable, and the research results have important academic and application value. Thus, this thesis has been highly praised by the eight Ph.D. thesis reviewers and it was rated as an outstanding doctoral dissertation by Peking University. As supervisors of Dr. Li, we are glad to recommend this thesis to readers, particularly those specialized or interested in the related areas.

Beijing
September 2015

Prof. Xing Zhang
Prof. Ru Huang

Abstract

With transistor dimension shrinking into nanoscale regime, it suffer from significant drive current reduction, due to mobility degradation and source/drain parasitic resistance increase. Further development of CMOS technology will strongly depend on the introduction of new material, new process, and new device structure. Germanium (Ge), owing to its high and more symmetric carrier mobility, is considered as a potential channel material for high-performance CMOS devices at 11 nm technology node and beyond. Although Ge pMOSFETs have shown excellent performance, some issues still need to be solved for realizing high performance Ge nMOSFETs, such as poor gate interface quality and large source/drain parasitic resistance. The large source/drain parasitic resistance is an important limiting factor for drive current enhancement of Ge nMOSFETs. Therefore, this thesis focuses on reducing the source/drain parasitic resistance and several feasible solutions have been proposed.

Schottky source/drain is a promising structure for Ge-based device, but the Fermi level pinning effect in metal/Ge contact severely impedes the performance improvement of Ge Schottky Barrier nMOSFET. Therefore, germanium-based Schottky barrier height (SBH) modulation technique is investigated in detail in this thesis. The implantation after germanide (IAG) technique is first proposed to modulate the electron SBH. Phosphorus (P) and arsenic (As) are chosen in the experiment and the influence of the drive-in annealing temperature, implantation dose, and implantation energy on electron SBH modulation is studied. Finally, a record-low electron SBH of 0.10 eV is achieved and good ohmic contact characteristic of NiGe/n-Ge diode is realized, which is promising to promote the performance of Ge-based Schottky barrier nMOSFET.

The self-aligned germanide process is critical to reduce source/drain parasitic resistance for Ge MOSFET, but the poor thermal stability of NiGe puts a roadblock for its application. Therefore, P and Sb co-implantation technique is first proposed in this thesis to improve the thermal stability of NiGe. With this technique, the surface morphology of NiGe film is well improved and the thermal stability of NiGe is at least enhanced to 600 °C. Besides, the electrical characteristic of NiGe/Ge diodes is also improved by this technique. Good ohmic contact characteristic of NiGe/n-Ge diode is also realized and the corresponding contact resistivity is dramatically reduced to 1.2 × 10^{-6} Ω cm^2. Finally, the P and Sb co-implantation technique is successfully integrated into Ge nMOSFET, and the devices show good output characteristics, which verify that the P and Sb co-implantation technique is favorable for promoting the performance of Ge nMOSFET.

The contact resistance in source/drain comprises the dominant component of parasitic resistance in sub-100 nm MOSFETs, but it is difficult to reduce the contact resistance in Ge-based nMOSFETs, partially due to the poor n-type dopant electrical concentration. Therefore, this thesis addresses the high contact resistance by enhancing the n-type dopant activation in Ge. By optimizing multiple implantation and multiple annealing (MIMA) technique, a high electrical activation over 1 × 10^{20} cm^{-3} is demonstrated, and the corresponding contact resistivity is reduced to 3.8 × 10^{-7} Ω cm^2. Meanwhile, the performance of Ge n^+/p diodes is also improved by the MIMA technique. The MIMA Ge n^+/p diodes exhibit an I_{on}/I_{off} ratio over 10^5, which is much better than the single implanted diode. Finally, the MIMA technique is successfully integrated into Ge nMOSFET, and the saturation current is increased by 6.7 %, which demonstrates that the parasitic resistance is effectively reduced by the MIMA technique.

Keywords Germanium-based MOSFET · Contact resistance · Dopant segregation · Nickel germanide · Dopant activation

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