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Richard Gaggl

# Delta-Sigma A/D-Converters

Practical Design for Communication  
Systems

 Springer

Richard Gaggl  
Design Center Villach  
Infineon Technologies  
Villach, Austria

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*For Tine, Marie and Anna*

# Preface

Analog and mixed-signal circuits continue to play a major role in modern technologies. Obviously, interfacing with antennas, wires, microphones and image sensors requires analog signal processing such as signal amplification, filtering and conversion from analog to digital. A/D-converters are bridges between the analog real world and the digital world. In practical applications the A/D-converters often become bottlenecks and their design is critical to overall system performance. Furthermore, the A/D-converters show a significant impact on system efficiency (power consumption), product costs (chip area) and robustness. Nevertheless, digital circuits drive the market such as microprocessors and system-on-chip solutions. The technology development has been optimized over the last decades to reduce the power consumption and chip area of digital circuits. Contrarily, the implementation of analog circuits has become more difficult using these modern semiconductor technologies. Smaller transistor sizes come along with a reduced tolerable voltage range resulting in a more challenging design. As a consequence, modern CMOS technologies drive the need for novel architectures to keep pace with improving efficiency of A/D-conversion.

The emphasis of this book is on practical design aspects for broadband analog-to-digital converters for communications. The embedded designs are employed for transceivers in the field of Asymmetric Digital Subscriber Line (ADSL) solutions and Wireless Local-Area Network (WLAN) applications. An area- and power-efficient realization of a converter is mandatory to remain competitive in the market. The right choice for the converter topology and architecture needs to be done very carefully to result in an attractive figure-of-merit (FOM). The book begins with a brief overview of basic concepts about ADSL and WLAN to understand the requirements on Analog-to-Digital (A/D) converters. In both fields of applications it will turn out that a delta-sigma approach is a good choice for fulfilling all requirements. At architecture level, issues on different modulator topologies are being discussed employing the provided technology node. The technology features influence the choice of different architectures in order to improve the circuit implementation. The design issues are pointed out in detail for modern digital Complementary Metal-Oxide-Semiconductor (CMOS) technologies, beginning with 180 nm and go-

ing down to 65 nm feature size. Beside practical aspects, challenges on mixed-signal design level are addressed to optimize the converters in terms of consumed chip area, power consumption and design for yield in high volume production. Thus, careful considerations on circuit- and architectural-level are done by introducing a dynamic-biasing technique, a feedforward-approach and a resolution in time instead of amplitude resolution. In 180 nm CMOS, a 85 dB dynamic range multi-bit delta-sigma A/D converter as well as in 130 nm CMOS, a power optimized 14 bit switched-capacitor delta-sigma modulator, are designed for ADSL applications, achieving  $1.8 \frac{\text{pJ}}{\text{conv}}$  and  $0.7 \frac{\text{pJ}}{\text{conv}}$ , respectively. In 65 nm CMOS, a design for a 10 bit delta-sigma converter with a signal bandwidth up to 20 MHz is presented for a baseband WLAN solution attaining  $0.15 \frac{\text{pJ}}{\text{conv}}$ . A new architecture is introduced by a time-encoding technique replacing a conventional amplitude quantization.

## Acknowledgements

The content of the book reflects my work as a mixed-signal design engineer in the former communications group at Infineon Technologies and my work as principal engineer at Lantiq, Villach, Austria. Furthermore, the content was enhanced during my stay at the Technical University of Graz, Austria, for working on my doctoral thesis. This book would not have been possible without the help and support from many people.

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Kärnten, Austria

Richard Gaggl



# Contents

<b>1</b>	<b>Introduction</b>	1
1.1	Motivation	1
1.2	Organization of This Book	2
1.3	Asymmetric Digital Subscriber Line	4
1.3.1	ADSL System Configuration	6
1.3.2	A/D-Converter Requirements for ADSL	7
1.4	Wireless Local-Area Network	8
1.4.1	WLAN 802.11n System Configuration	11
1.4.2	A/D-Converter Requirements for WLAN 802.11n	13
<b>2</b>	<b>Limitations of Delta-Sigma Converters</b>	15
2.1	Basics of A/D-Conversion	15
2.2	Main A/D-Converter Specifications	18
2.3	Delta-Sigma Converter	22
2.3.1	Single-Loop Modulator	24
2.3.2	Cascaded-Loop Modulator	27
2.3.3	Discrete-Time vs. Continuous-Time Loopfilter	29
2.3.4	Circuit Nonidealities for Discrete-Time Loopfilters	30
2.3.5	Circuit Nonidealities for Continuous-Time Loopfilters	34
2.3.6	Design Methodology for CT-Modulators	38
2.3.7	Summary of Delta-Sigma Converter	40
2.4	Asynchronous Delta-Sigma Modulation	41
2.4.1	Spectral Analysis of Duty-Cycle Modulation	43
2.4.2	An Asynchronous Delta-Sigma Modulator	44
2.4.3	Summary of Asynchronous Delta-Sigma Modulation	47
2.5	Impact on Jitter	48
2.5.1	Jitter Definition	48
2.5.2	SNR vs. Jitter of Sampled Signals	49
2.6	Conclusion	52
<b>3</b>	<b>A Delta-Sigma Converter with Dynamic-Biasing Technique</b>	55
3.1	Architectural Considerations	56

3.1.1	Considerations on Signal-to-Noise Ratio . . . . .	57
3.2	Circuit-Design . . . . .	59
3.2.1	Clocking-Scheme . . . . .	60
3.2.2	Switched-Capacitor Integrator . . . . .	60
3.2.3	Quantizer . . . . .	63
3.2.4	Reference Buffer . . . . .	63
3.2.5	Operational-Amplifier . . . . .	64
3.3	Measurement Results . . . . .	68
3.4	Conclusion . . . . .	73
<b>4</b>	<b>A Feed-Forward Delta-Sigma Converter for ADSL . . . . .</b>	<b>75</b>
4.1	Architectural Considerations . . . . .	76
4.1.1	A Feed-Forward Approach . . . . .	76
4.2	Circuit-Design . . . . .	80
4.2.1	Operational-Transconductance-Amplifier . . . . .	81
4.2.2	Second-Integrator and 3 Bit-Quantizer . . . . .	83
4.2.3	Reference Buffer in Open-Loop Configuration . . . . .	84
4.3	Measurement Results . . . . .	84
4.4	Conclusion . . . . .	87
<b>5</b>	<b>A Delta-Sigma Converter for WLAN Using a TEQ . . . . .</b>	<b>89</b>
5.1	The Principle of a Time-Encoding Quantizer . . . . .	90
5.2	System-Design Considerations . . . . .	94
5.2.1	Integration of a TEQ into a Delta-Sigma Modulator . . . . .	94
5.2.2	Design-Specifications and System-Level Design . . . . .	95
5.2.3	Architecture for A/D-Converter . . . . .	98
5.3	Circuit Design . . . . .	100
5.3.1	Loopfilter . . . . .	100
5.3.2	Integrator-Stage and Operational-Amplifier . . . . .	102
5.3.3	Time-Encoding Quantizer . . . . .	103
5.3.4	Comparator . . . . .	104
5.3.5	D/A-Converter in Feedback-Path . . . . .	105
5.3.6	Overall Circuit of A/D-Converter . . . . .	107
5.4	Measurement Results . . . . .	110
5.4.1	Measurement Setup . . . . .	113
5.4.2	Measurement of PSD-Plots . . . . .	116
5.5	Digital Decimation Filter . . . . .	122
5.6	Conclusion . . . . .	124
<b>6</b>	<b>Conclusions . . . . .</b>	<b>127</b>
6.1	Research Work Overview . . . . .	127
6.2	Figure-of-Merit Comparison . . . . .	129
6.3	Outlook on Future Trends in Delta-Sigma Design . . . . .	135
	<b>Bibliography . . . . .</b>	<b>139</b>
	<b>Index . . . . .</b>	<b>143</b>

# List of Notations

## *Acronymus and Abbreviations*

<b>ADSL</b>	Asymmetric Digital Subscriber Line
<b>ADSL2+</b>	Asymmetric Digital Subscriber Line 2+
<b>A/D</b>	Analog-to-Digital
<b>ADC</b>	Analog-to-Digital Converter
<b>AFE</b>	Analog Front End
<b>ASIC</b>	Application-Specific Integrated Circuit
<b>BSS</b>	Basic Service Set
<b>CMOS</b>	Complementary Metal-Oxide-Semiconductor
<b>CO</b>	Central Office
<b>conv</b>	conversion
<b>CPE</b>	Customer Premises Equipment
<b>CT</b>	Continuous Time
<b>DAC</b>	Digital-to-Analog Converter
<b>D/A</b>	Digital-to-Analog
<b>DC</b>	Direct Current
<b>DEM</b>	Dynamic Element Matching
<b>DLC</b>	Digital Loop Carrier
<b>DMT</b>	Discrete Multi-Tone
<b>DNL</b>	Differential Non-Linearity
<b>DR</b>	Dynamic Range
<b>DSL</b>	Digital Subscriber Line
<b>DSSS</b>	Direct-Sequence Spread-Spectrum
<b>DT</b>	Discrete Time
<b>ELD</b>	Excess Loop Delay
<b>ENOB</b>	Effective Number-of-Bits
<b>FET</b>	Field-Effect Transistor
<b>FFT</b>	Fast Fourier Transform
<b>FHSS</b>	Frequency-Hopping Spread-Spectrum
<b>FIR</b>	Finite Impulse Response

<b>FOM</b>	Figure Of Merit
<b>GBW</b>	Gain-BandWidth Product
<b>GOX</b>	Gate-Oxide
<b>HDSL</b>	High bit-rate Digital Subscriber Line
<b>IBQN</b>	In-Band Quantization Noise
<b>ICN</b>	Idle Channel Noise
<b>IEEE</b>	Institute of Electrical and Electronics Engineers
<b>INL</b>	Integral Non-Linearity
<b>ISDN</b>	Integrated Service Digital Network
<b>ITU-T</b>	International Telecommunications Union-Standardization Sector
<b>JFET</b>	Junction Field-Effect Transistor
<b>LAN</b>	Local-Area Network
<b>MAC</b>	Media Access Control
<b>MASH</b>	Multi-stage noise-Shaping
<b>MOSFET</b>	Metal-Oxide-Semiconductor Field-Effect Transistor
<b>MTPR</b>	Missing-Tone Power Ratio
<b>NTF</b>	Noise Transfer Function
<b>OFDM</b>	Orthogonal Frequency-Division Multiplexing
<b>OpAmp</b>	Operational Amplifier
<b>OSI</b>	Open System Interconnection
<b>OSR</b>	Over-Sampling Ratio
<b>OTA</b>	Operational Transconductance Amplifier
<b>PLL</b>	Phase-Locked Loop
<b>POTS</b>	Plain-Old Telephone Service
<b>PSD</b>	Power Spectral Density
<b>PSTN</b>	Public Switched Telephone Network
<b>PWM</b>	Pulse-Width Modulation
<b>RAM</b>	Random-Access Memory
<b>rms</b>	root mean square
<b>ROSR</b>	Ratio-OSR
<b>SAR</b>	Successive Approximation Register ADC
<b>SC</b>	Switched-Capacitor
<b>SFDR</b>	Spurious-Free Dynamic Range
<b>S/H</b>	Sample-and-Hold
<b>SNDR</b>	Signal-to-Noise and Distortion Ratio
<b>SNR</b>	Signal-to-Noise Ratio
<b>SoC</b>	System on Chip
<b>SPICE</b>	Simulation Program with Integrated Circuit Emphasis
<b>SQNR</b>	Signal-to-Quantization-Noise Ratio
<b>STF</b>	Signal Transfer Function
<b>TCP/IP</b>	Transmission Control Protocol/Internet Protocol
<b>TDC</b>	Time-to-Digital Converter
<b>TEM</b>	Time-Encoding Machine
<b>TEQ</b>	Time-Encoding Quantizer

<b>THD</b>	Total Harmonic Distortion
<b>VLSI</b>	Very Large-Scale Integrated Circuits
<b>WLAN</b>	Wireless Local-Area Network

*Physical Symbols*

$C$	Capacitance [F]
$f$	Frequency [Hz]
$K$	Boltzmann's constant ( $1.38 \times 10^{-23}$ ) [J/K]
$I$	Current [A]
$P$	Power (dissipation) [W]
$R$	Resistance [ $\Omega$ ]
$t$	Time [s]
$T$	Absolute temperature [K]
$V$	Voltage [V]

*Electrical Symbols*

$\alpha$	(Relativ) pulse width [-]
$a_i$	Polynomial coefficient [-]
$A_{max}$	Amplitude of a sinusoidal signal [V]
$A_0$	Finite OTA or OpAmp gain at DC [dB]
$B$	Number of quantization bits [-]
$BW$	Bandwidth [Hz]
$C$	Number of relevant clock edges within one period ( $C = 1$ or $C = 2$ ) [-]
$C_{eq}$	Equivalent capacitance [F]
$C_I$	Integrator capacitance [F]
$C_L$	Load capacitance [F]
$C_P$	Parasitic capacitance [F]
$C_S$	Sampling capacitance [F]
$conv$	Conversion [-]
$\Delta$	Quantizer step size [V]
$\Delta_3$	Distortion coefficient [-]
$e(n)$	Discrete-time error signal [V]
$E(z)$	Discrete-time quantization error in $z$ -domain [V]
$E_1(z)$	Discrete-time quantization error in $z$ -domain of first quantizer [V]
$E_2(z)$	Discrete-time quantization error in $z$ -domain of second quantizer [V]
$f_B$	Analog signal bandwidth [Hz]
$f_S$	Sampling frequency [Hz]
$f_N$	Nyquist frequency [Hz]
$f_{sig}$	Signal frequency [Hz]
$G_E$	Gain Error of an integrator [dB]
$g_{lp}$	Gain of a lowpass filter [-]
$g_m$	Transconductance of a transistor [A/V]
$g_o$	Output conductance of a transistor [A/V]
$H_D(z)$	Discrete-time transfer function of a digital filter [-]
$H_{OP}(s)$	Continuous-time transfer function of an OpAmp [-]

$H(s)$	Continuous-time (loop-filter) transfer function [-]
$H(z)$	Discrete-time (loop-filter) transfer function [-]
$\Im\{H(j\omega)\}$	Complex part of transfer function $H(j\omega)$ [-]
$h_a(t)$	Continuous time (analog) impulse response [V]
$h_d[n]$	Discrete time (digital) impulse response [V]
$J_p(x)$	Bessel function of the first kind and order $p$ [-]
$k$	Index number [-]
$k_g$	Coefficient for gain-scaling [-]
$K'$	Gain factor of a MOS-device [ $A/V^2$ ]
$K_c$	Unity gain frequency of an integrator [Hz]
$\lambda_1$	Capacitive feedback factor during sampling phase [-]
$\lambda_2$	Capacitive feedback factor during integrating phase [-]
$L$	Length of a MOS-device [m]
$L$	Order of loop filter in a delta-sigma modulator [-]
$L^{-1}\{H(s)\}$	Inverse Laplace transformation of $H(s)$ [-]
$\mu$	Frequency of modulating input signal for PWM [Hz]
$m$	Index number [-]
$N$	Number of bits of a quantizer [-]
$\phi(f)$	Phase noise density [ $V^2/Hz$ ]
$\phi_1$	First (sampling) phase of switched capacitor circuit [-]
$\phi_{1d}$	First (sampling) delayed phase of switched capacitor circuit [-]
$\phi_2$	Second (integrating) phase of switched capacitor circuit [-]
$\phi_{2d}$	Second (integrating) delayed phase of switched capacitor circuit [-]
$p(t)$	Continuous-time pulse [V]
$p_i$	Frequency of a pole [Hz]
$\hat{P}$	Amplitude of pulse $p(t)$ [V]
$\omega$	Angular frequency [rad/s]
$\omega_0$	Center frequency [rad/s]
$\omega_c$	Carrier frequency [rad/s]
$\omega_D$	Dominant pole frequency of an OpAmp [rad/s]
$\omega_{lp}$	Pole frequency of a lowpass filter [rad/s]
$\omega_{osc}$	Limit-cycle frequency within an oscillating PWM loop [rad/s]
$\omega_{sig}$	Signal Frequency [rad/s]
$\hat{P}$	Amplitude of a square waveform [V]
$P_N$	Noise power [W]
$Q$	Quality factor of a pole or zero [-]
$\Re\{H(j\omega)\}$	Real part of transfer function $H(j\omega)$ [-]
$r_x(0)$	Autocorrelation function of function $x$ at zero [-]
$r_{ij}(0)$	Autocorrelation function of jitter function $t_j$ at zero [-]
$R_I$	Input resistance [ $\Omega$ ]
$R_L$	Load resistance [ $\Omega$ ]
$R_{on}$	Channel-resistance of a MOS in linear region [ $\Omega$ ]
$R_{sw}$	On-resistance of a closed switch [ $\Omega$ ]
$\rho_1$	Static error for closed loop configuration [-]
$\rho_2$	Static error for closed loop configuration [-]

$s$	Laplace-domain variable [rad/s]
$s_{LP}$	Parasitic pole frequency of a real integrator [rad/s]
$S_A(f)$	Power spectral density of the analog signal [W/Hz]
$S_e(f)$	Power spectral density of the error (quantization) noise [W/Hz]
$S_\phi(f)$	Power spectral density of the phase noise [W/Hz]
$S_q(f)$	Power spectral density of the shaped quantization noise [W/Hz]
$S_{ij}(f)$	Power spectral density of the jitter function [W/Hz]
$\sigma_{abs}$	Absolute Jitter [s]
$\sigma_{acc}(m)$	Accumulated jitter [s]
$\sigma_e^2$	Variance of uniformly distributed (interpolation) error [V <sup>2</sup> ]
$\sigma_{lt}$	Long-term jitter [s]
$\sigma_{per}$	Period Jitter [s]
$\sigma_q^2$	Variance of uniformly distributed quantization error [V <sup>2</sup> ]
$SNR_j$	Signal-to-noise ratio due to sampling with clock jitter [-]
$t_j$	Jitter function (time discrete random process) [-]
$T$	Signal period [s]
$T_c$	Limit-cycle period [s]
$T_{osc}$	Limit-cycle period within an oscillating PWM loop [s]
$T_s$	Sampling period [s]
$T_{sig}$	Signal period [s]
$T[k]$	Irregularly sampling sequence [-]
$u(t)$	Continuous-time signal [V]
$\hat{U}$	Amplitude sinusoidal signal [V]
$v$	Variable voltage [V]
$v_m$	Voltage amplitude [V]
$V_D$	Node voltage at drain of a MOS device [V]
$V_G$	Node voltage at gate of a MOS device [V]
$V_i$	Input (node) voltage [V]
$V_o$	Output (node) voltage [V]
$V_{ref}$	Provided reference voltage for A/D conversion [V]
$V_S$	Node voltage at source of a MOS device [V]
$V_{th}$	Threshold voltage of a MOS-device [V]
$w(t)$	Continuous-time signal [V]
$W$	Width of a MOS-device [m]
$x[m]$	Regularly sampled signal [V]
$x(n)$	Discrete-time (input) signal [V]
$x(t)$	Continuous-time (input) signal [V]
$x(T[k])$	Irregularly sampled signal [V]
$X(z)$	Discrete-time (input) signal in $z$ -domain [V]
$y(n)$	Discrete-time (output) signal [V]
$y(t)$	Continuous-time (output) signal [V]
$Y(z)$	Discrete-time (output) signal in $z$ -domain [V]
$Y_1(z)$	Discrete-time (output) signal in $z$ -domain of first stage [V]
$Y_2(z)$	Discrete-time (output) signal in $z$ -domain of second stage [V]

$z$	Discrete-time frequency variable in $z$ -domain, $z = e^{sT_s}$ [V]
$z_i$	Frequency of a zero [rad/s]
$Z\{h_d[n]\}$	$z$ -transformation of $h_d[n]$ [-]
$Z^{-1}\{H(z)\}$	Inverse $z$ -transformation of $H(z)$ [-]