Springer Series in Advanced Microelectronics

Volume 39

For further volumes:
www.springer.com/series/4076

The Springer Series in Advanced Microelectronics provides systematic information on all the topics relevant for the design, processing, and manufacturing of microelectronic devices. The books, each prepared by leading researchers or engineers in their fields, cover the basic and advanced aspects of topics such as wafer processing, materials, device design, device technologies, circuit design, VLSI implementation, and subsystem technology. The series forms a bridge between physics and engineering and the volumes will appeal to practicing engineers as well as research scientists.

Richard Gaggl

Delta-Sigma A/D-Converters

Practical Design for Communication Systems

Springer

Richard Gaggl
Design Center Villach
Infineon Technologies
Villach, Austria

ISSN 1437-0387 Springer Series in Advanced Microelectronics
ISBN 978-3-642-34542-5 ISBN 978-3-642-34543-2 (eBook)
DOI 10.1007/978-3-642-34543-2
Springer Heidelberg New York Dordrecht London

Library of Congress Control Number: 2012953283

Printed on acid-free paper

Springer is part of Springer Science+Business Media (www.springer.com)

For Tine, Marie and Anna

Preface

Analog and mixed-signal circuits continue to play a major role in modern technologies. Obviously, interfacing with antennas, wires, microphones and image sensors requires analog signal processing such as signal amplification, filtering and conversion from analog to digital. A/D-converters are bridges between the analog real world and the digital world. In practical applications the A/D-converters often become bottlenecks and their design is critical to overall system performance. Furthermore, the A/D-converters show a significant impact on system efficiency (power consumption), product costs (chip area) and robustness. Nevertheless, digital circuits drive the market such as microprocessors and system-on-chip solutions. The technology development has been optimized over the last decades to reduce the power consumption and chip area of digital circuits. Contrarily, the implementation of analog circuits has become more difficult using these modern semiconductor technologies. Smaller transistor sizes come along with a reduced tolerable voltage range resulting in a more challenging design. As a consequence, modern CMOS technologies drive the need for novel architectures to keep pace with improving efficiency of A/D-conversion.

The emphasis of this book is on practical design aspects for broadband analog-to-digital converters for communications. The embedded designs are employed for transceivers in the field of Asymmetric Digital Subscriber Line (ADSL) solutions and Wireless Local-Area Network (WLAN) applications. An area- and power-efficient realization of a converter is mandatory to remain competitive in the market. The right choice for the converter topology and architecture needs to be done very carefully to result in an attractive figure-of-merit (FOM). The book begins with a brief overview of basic concepts about ADSL and WLAN to understand the requirements on Analog-to-Digital (A/D) converters. In both fields of applications it will turn out that a delta-sigma approach is a good choice for fulfilling all requirements. At architecture level, issues on different modulator topologies are being discussed employing the provided technology node. The technology features influence the choice of different architectures in order to improve the circuit implementation. The design issues are pointed out in detail for modern digital Complementary Metal-Oxide-Semiconductor (CMOS) technologies, beginning with 180 nm and go-

ing down to 65 nm feature size. Beside practical aspects, challenges on mixed-signal design level are addressed to optimize the converters in terms of consumed chip area, power consumption and design for yield in high volume production. Thus, careful considerations on circuit- and architectural-level are done by introducing a dynamic-biasing technique, a feedforward-approach and a resolution in time instead of amplitude resolution. In 180 nm CMOS, a 85 dB dynamic range multi-bit delta-sigma A/D converter as well as in 130 nm CMOS, a power optimized 14 bit switched-capacitor delta-sigma modulator, are designed for ADSL applications, achieving 1.8 $\frac{\text{pJ}}{\text{conv}}$ and 0.7 $\frac{\text{pJ}}{\text{conv}}$, respectively. In 65 nm CMOS, a design for a 10 bit delta-sigma converter with a signal bandwidth up to 20 MHz is presented for a baseband WLAN solution attaining 0.15 $\frac{\text{pJ}}{\text{conv}}$. A new architecture is introduced by a time-encoding technique replacing a conventional amplitude quantization.

Acknowledgements

The content of the book reflects my work as a mixed-signal design engineer in the former communications group at Infineon Technologies and my work as principal engineer at Lantiq, Villach, Austria. Furthermore, the content was enhanced during my stay at the Technical University of Graz, Austria, for working on my doctoral thesis. This book would not have been possible without the help and support from many people.

There are many people to thank for supporting the work that has been compressed into this book. At this point, I would like to thank the people who directly contributed to the content of this book. First of all, I owe deep gratitude to Prof. Dr. Wolfgang Pribyl for inspiration and the initial encouragement to carry out this book, as well as his supervision and help during my stay at the Technical University of Graz. I am deeply indebted to my co-supervisor Prof. Dr. Willy Sansen from the Katholieke University Leuven whose help, stimulating suggestions on all technical aspects and encouragement helped me in all the time of research for and on the general style of writing the manuscript. Furthermore, I would like to thank Assoc. Prof. Dr. Luis Hernandez, Assoc. Prof. Dr. Susana Paton and Ass. Prof. Dr. Enrique Prefasi, all from the University Madrid, for their stimulating ideas and academic background investigations on time-encoding quantizers.

I would like to thank both companies Infineon Technologies and Lantiq for allowing me to concentrate the results of several years of working experience in this exciting field into a volume for the series of Advanced Microelectronics. Thanks to my colleagues from the communications department for their help with design, layout and measurements on my three test-chips. I want to thank them for all their help, support, interest and valuable hints. Further on, I especially want to thank Dr. Andreas Wiesbauer for his great help with oversampling converters as well as Dr. Dietmar Sträußnigg for his support in control engineering and the needed boost throughout my work.

Lastly, and most importantly, I would like to give my special thanks to my whole family. Especially, I wish to express my gratitude to my wife Tine and my daughters

Marie and Anna whose patient love enabled me to complete this work and for their understanding of my absence during long working weekends. To them I dedicate this book.

Kärnten, Austria Richard Gaggl

Contents

List of Notations

Acronymus and Abbreviations

ADSL	Asymmetric Digital Subscriber Line
ADSL2+	Asymmetric Digital Subscriber Line 2+
A/D	Analog-to-Digital
ADC	Analog-to-Digital Converter
AFE	Analog Front End
ASIC	Application-Specific Integrated Circuit
BSS	Basic Service Set
CMOS	Complementary Metal-Oxide-Semiconductor
CO	Central Office
conv	conversion
CPE	Customer Premises Equipment
CT	Continuous Time
DAC	Digital-to-Analog Converter
D/A	Digital-to-Analog
DC	Direct Current
DEM	Dynamic Element Matching
DLC	Digital Loop Carrier
DMT	Discrete Multi-Tone
DNL	Differential Non-Linearity
DR	Dynamic Range
DSL	Digital Subscriber Line
DSSS	Direct-Sequence Spread-Spectrum
DT	Discrete Time
ELD	Excess Loop Delay
ENOB	Effective Number-of-Bits
FET	Field-Effect Transistor
FFT	Fast Fourier Transform
FHSS	Frequency-Hopping Spread-Spectrum
FIR	Finite Impulse Response

FOM	Figure Of Merit
GBW	Gain-BandWidth Product
GOX	Gate-Oxide
HDSL	High bit-rate Digital Subscriber Line
IBQN	In-Band Quantization Noise
ICN	Idle Channel Noise
IEEE	Institute of Electrical and Electronics Engineers
INL	Integral Non-Linearity
ISDN	Integrated Service Digital Network
ITU-T	International Telecommunications Union-Standardization Sector
JFET	Junction Field-Effect Transistor
LAN	Local-Area Network
MAC	Media Access Control
MASH	Multi-stAge noise-SHaping
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MTPR	Missing-Tone Power Ratio
NTF	Noise Transfer Function
OFDM	Orthogonal Frequency-Division Multiplexing
OpAmp	Operational Amplifier
OSI	Open System Interconnection
OSR	Over-Sampling Ratio
OTA	Operational Transconductance Amplifier
PLL	Phase-Locked Loop
POTS	Plain-Old Telephone Service
PSD	Power Spectral Density
PSTN	Public Switched Telephone Network
PWM	Pulse-Width Modulation
RAM	Random-Access Memory
rms	root mean square
ROSR	Ratio-OSR
SAR	Successive Approximation Register ADC
SC	Switched-Capacitor
SFDR	Spurious-Free Dynamic Range
S/H	Sample-and-Hold
SNDR	Signal-to-Noise and Distortion Ratio
SNR	Signal-to-Noise Ratio
SoC	System on Chip
SPICE	Simulation Program with Integrated Circuit Emphasis
SQNR	Signal-to-Quantization-Noise Ratio
STF	Signal Transfer Function
TCP/IP	Transmission Control Protocol/Internet Protocol
TDC	Time-to-Digital Converter
TEM	Time-Encoding Machine
TEQ	Time-Encoding Quantizer

THD	Total Harmonic Distortion
VLSI	Very Large-Scale Integrated Circuits
WLAN	Wireless Local-Area Network

Physical Symbols

C	Capacitance [F]
f	Frequency [Hz]
K	Boltzmann's constant (1.38×10^{-23}) [J/K]
I	Current [A]
P	Power (dissipation) [W]
R	Resistance [Ω]
t	Time [s]
T	Absolute temperature [K]
V	Voltage [V]

Electrical Symbols

α	(Relativ) pulse width [–]
a_i	Polynomial coefficient [–]
A_{max}	Amplitude of a sinusoidal signal [V]
A_0	Finite OTA or OpAmp gain at DC [dB]
B	Number of quantization bits [–]
BW	Bandwidth [Hz]
C	Number of relevant clock edges within one period ($C = 1$ or $C = 2$) [–]
C_{eq}	Equivalent capacitance [F]
C_I	Integrator capacitance [F]
C_L	Load capacitance [F]
C_P	Parasitic capacitance [F]
C_S	Sampling capacitance [F]
$conv$	Conversion [–]
Δ	Quantizer step size [V]
Δ_3	Distortion coefficient [–]
$e(n)$	Discrete-time error signal [V]
$E(z)$	Discrete-time quantization error in z-domain [V]
$E_1(z)$	Discrete-time quantization error in z-domain of first quantizer [V]
$E_2(z)$	Discrete-time quantization error in z-domain of second quantizer [V]
f_B	Analog signal bandwidth [Hz]
f_S	Sampling frequency [Hz]
f_N	Nyquist frequency [Hz]
f_{sig}	Signal frequency [Hz]
G_E	Gain Error of an integrator [dB]
g_{lp}	Gain of a lowpass filter [–]
g_m	Transconductance of a transistor [A/V]
g_o	Output conductance of a transistor [A/V]
$H_D(z)$	Discrete-time transfer function of a digital filter [–]
$H_{OP}(s)$	Continuous-time transfer function of an OpAmp [–]

$H(s)$	Continuous-time (loop-filter) transfer function [–]
$H(z)$	Discrete-time (loop-filter) transfer function [–]
$\Im\{H(j\omega)\}$	Complex part of transfer function $H(j\omega)$ [–]
$h_a(t)$	Continuous time (analog) impulse response [V]
$h_d[n]$	Discrete time (digital) impulse response [V]
$J_p(x)$	Bessel function of the first kind and order p [–]
k	Index number [–]
k_g	Coefficient for gain-scaling [–]
K'	Gain factor of a MOS-device [A/V^2]
K_c	Unity gain frequency of an integrator [Hz]
λ_1	Capacitive feedback factor during sampling phase [–]
λ_2	Capacitive feedback factor during integrating phase [–]
L	Length of a MOS-device [m]
L	Order of loop filter in a delta-sigma modulator [–]
$L^{-1}\{H(s)\}$	Inverse Laplace transformation of $H(s)$ [–]
μ	Frequency of modulating input signal for PWM [Hz]
m	Index number [–]
N	Number of bits of a quantizer [–]
$\phi(f)$	Phase noise density [V^2/Hz]
ϕ_1	First (sampling) phase of switched capacitor circuit [–]
ϕ_{1d}	First (sampling) delayed phase of switched capacitor circuit [–]
ϕ_2	Second (integrating) phase of switched capacitor circuit [–]
ϕ_{2d}	Second (integrating) delayed phase of switched capacitor circuit [–]
$p(t)$	Continuous-time pulse [V]
p_i	Frequency of a pole [Hz]
$\hat{P}$	Amplitude of pulse $p(t)$ [V]
ω	Angular frequency [rad/s]
ω_0	Center frequency [rad/s]
ω_c	Carrier frequency [rad/s]
ω_D	Dominant pole frequency of an OpAmp [rad/s]
ω_{lp}	Pole frequency of a lowpass filter [rad/s]
ω_{osc}	Limit-cycle frequency within an oscillating PWM loop [rad/s]
ω_{sig}	Signal Frequency [rad/s]
$\hat{P}$	Amplitude of a square waveform [V]
P_N	Noise power [W]
Q	Quality factor of a pole or zero [–]
$\Re\{H(j\omega)\}$	Real part of transfer function $H(j\omega)$ [–]
$r_x(0)$	Autocorrelation function of function x at zero [–]
$r_{tj}(0)$	Autocorrelation function of jitter function t_j at zero [–]
R_I	Input resistance [Ω]
R_L	Load resistance [Ω]
Ron	Channel-resistance of a MOS in linear region [Ω]
Rsw	On-resistance of a closed switch [Ω]
ρ_1	Static error for closed loop configuration [–]
ρ_2	Static error for closed loop configuration [–]

s	Laplace-domain variable [rad/s]
s_{LP}	Parasitic pole frequency of a real integrator [rad/s]
$S_A(f)$	Power spectral density of the analog signal [W/Hz]
$S_e(f)$	Power spectral density of the error (quantization) noise [W/Hz]
$S_\phi(f)$	Power spectral density of the phase noise [W/Hz]
$S_q(f)$	Power spectral density of the shaped quantization noise [W/Hz]
$S_{tj}(f)$	Power spectral density of the jitter function [W/Hz]
σ_{abs}	Absolute Jitter [s]
$\sigma_{acc}(m)$	Accumulated jitter [s]
σ_e^2	Variance of uniformly distributed (interpolation) error [V^2]
σ_{lt}	Long-term jitter [s]
σ_{per}	Period Jitter [s]
σ_q^2	Variance of uniformly distributed quantization error [V^2]
SNR_j	Signal-to-noise ratio due to sampling with clock jitter [–]
t_j	Jitter function (time discrete random process) [–]
T	Signal period [s]
T_c	Limit-cycle period [s]
T_{osc}	Limit-cycle period within an oscillating PWM loop [s]
T_s	Sampling period [s]
T_{sig}	Signal period [s]
$T[k]$	Irregularly sampling sequence [–]
$u(t)$	Continuous-time signal [V]
$\hat{U}$	Amplitude sinusoidal signal [V]
v	Variable voltage [V]
v_m	Voltage amplitude [V]
V_D	Node voltage at drain of a MOS device [V]
V_G	Node voltage at gate of a MOS device [V]
V_i	Input (node) voltage [V]
V_o	Output (node) voltage [V]
V_{ref}	Provided reference voltage for A/D conversion [V]
V_S	Node voltage at source of a MOS device [V]
Vth	Threshold voltage of a MOS-device [V]
$w(t)$	Continuous-time signal [V]
W	Width of a MOS-device [m]
$x[m]$	Regularly sampled signal [V]
$x(n)$	Discrete-time (input) signal [V]
$x(t)$	Continuous-time (input) signal [V]
$x(T[k])$	Irregularly sampled signal [V]
$X(z)$	Discrete-time (input) signal in z-domain [V]
$y(n)$	Discrete-time (output) signal [V]
$y(t)$	Continuous-time (output) signal [V]
$Y(z)$	Discrete-time (output) signal in z-domain [V]
$Y_1(z)$	Discrete-time (output) signal in z-domain of first stage [V]
$Y_2(z)$	Discrete-time (output) signal in z-domain of second stage [V]

z	Discrete-time frequency variable in z-domain, $z = e^{sT_S}$ [V]
z_i	Frequency of a zero [rad/s]
$Z\{h_d[n]\}$	z-transformation of $h_d[n]$ [–]
$Z^{-1}\{H(z)\}$	Inverse z-transformation of $H(z)$ [–]