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Reconfigurable Computing: Architectures, Tools and Applications

4th International Workshop, ARC 2008
London, UK, March 26-28, 2008
Proceedings

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Preface

For many years, the idea of reconfigurable hardware systems has represented the *Holy Grail* for computer system designers. It has been recognized for a long time that the microprocessor provides high flexibility but at a very low performance merit in terms of MIPS/W or other such measures. *Reconfigurable systems* are thus attractive as they can be configured to provide the best match for the computational requirements at that specific time, giving much better area – speed – power performance.

However, the practicalities of achieving such a reconfigurable system are numerous and require the development of: suitable reconfigurable hardware to support the dynamic behavior; programming tools to allow the dynamic behavior of the reconfigurability to be modelled; programming languages to support reconfiguration; and verification techniques that can demonstrate that reconfiguration has happened correctly at each stage. While the problems are many, the existence and development of technologies such as the multi-core processor architecture, reconfigurable computing architectures, and application-specific processors suggest there is a strong desire for reconfigurable systems. Moreover, FPGAs also provide the ideal platforms for the development of such platforms.

The major motivation behind the International Workshop on Applied Reconfigurable Computing (ARC) series is to create a forum for presenting and discussing on-going research efforts in applied reconfigurable computing. The workshop also focuses on compiler and mapping techniques, and new reconfigurable computing architectures. The series of editions started in 2005 in Algarve, Portugal, followed by the 2006 workshop in Delft, The Netherlands, and last year's workshop in Mangaratiba, Rio de Janeiro, Brazil. As in previous years, selected papers have been published as a Springer LNCS (*Lecture Notes in Computer Science*) volume.

This LNCS volume includes the papers selected for the fourth edition of the Workshop (ARC 2008), held at Imperial College London, UK during March 26–28, 2008. The workshop attracted a large number of very good papers, describing interesting work on reconfigurable computing related subjects. A total of 56 papers were submitted to the workshop from 18 countries: UK (9), Republic of China (6), Germany (6), USA (5), The Netherlands (4), France (4), Greece (3), Portugal (3), Brazil (3), Republic of South Korea (2), Japan (2), Spain (2), Poland (2), India (1), Belgium (1), Turkey (1), Thailand (1) and Canada (1).

In most cases, submitted papers were evaluated by at least three members of the Program Committee. After careful selection, 21 papers were accepted as full papers (acceptance rate of 38.1%) and 14 as short papers (global acceptance rate of 63.6%). Those accepted papers led to a very interesting workshop program, which we consider to constitute a representative overview of on-going research efforts in reconfigurable computing, a rapidly evolving and maturing field.

Several people contributed to the success of the 2008 edition of the workshop. We would like to acknowledge the support of all the members of this year's workshop Steering and Program Committees in reviewing papers, in helping the paper selection, and in giving valuable suggestions. Special thanks also to the additional researchers who contributed to the reviewing process, to all the authors that submitted papers to the workshop, and to all the workshop attendees. Last but not least, we would like to thank Springer, and Alfred Hofmann in particular, for their continued support in publishing the proceedings as part of the LNCS series and to Jürgen Becker from the University of Karlsruhe for his continued support role.

January 2008

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Table of Contents

Keynotes

| | |
|--|---|
| Synthesizing FPGA Circuits from Parallel Programs | 1 |
| <i>Satnam Singh and David Greaves</i> | |
| From Silicon to Science: The Long Road to Production Reconfigurable Supercomputing | 2 |
| <i>Keith Underwood</i> | |
| The von Neumann Syndrome and the CS Education Dilemma | 3 |
| <i>Reiner Hartenstein</i> | |

Programming and Compilation

| | |
|---|----|
| Optimal Unroll Factor for Reconfigurable Architectures | 4 |
| <i>Ozana Silvia Dragomir, Elena Moscu-Panainte, Koen Bertels, and Stephan Wong</i> | |
| Programming Reconfigurable Decoupled Application Control Accelerator for Mobile Systems | 15 |
| <i>Samar Yazdani, Joël Cambonie, and Bernard Pottier</i> | |

DNA and String Processing Applications

| | |
|--|----|
| DNA Physical Mapping on a Reconfigurable Platform | 27 |
| <i>Adriano Idalgo and Nahri Moreano</i> | |
| Hardware BLAST Algorithms with Multi-seeds Detection and Parallel Extension | 39 |
| <i>Fei Xia, Yong Dou, and Jinbo Xu</i> | |
| Highly Space Efficient Counters for Perl Compatible Regular Expressions in FPGAs | 51 |
| <i>Chia-Tien Dan Lo and Yi-Gang Tai</i> | |

Scientific Applications

| | |
|---|----|
| A Custom Processor for a TDMA Solver in a CFD Application | 63 |
| <i>Filipe Oliveira, C. Silva Santos, F.A. Castro, and José C. Alves</i> | |
| A High Throughput FPGA-Based Floating Point Conjugate Gradient Implementation | 75 |
| <i>Antonio Roldao Lopes and George A. Constantinides</i> | |

Reconfigurable Computing Hardware and Systems

| | |
|--|-----|
| Physical Design of FPGA Interconnect to Prevent Information Leakage | 87 |
| <i>Sumanta Chaudhuri, Sylvain Guilley, Philippe Hoogvorst, Jean-Luc Danger, Taha Beyrouthy, Alin Razafindraibe, Laurent Fesquet, and Marc Renaudin</i> | |
| Symmetric Multiprocessor Design for Hybrid CPU/FPGA SoCs | 99 |
| <i>Shane Santner, Wesley Peck, Jason Agron, and David Andrews</i> | |
| Run-Time Adaptable Architectures for Heterogeneous Behavior Embedded Systems | 111 |
| <i>Antonio Carlos S. Beck, Mateus B. Rutzig, Georgi Gaydadjiev, and Luigi Carro</i> | |

Image Processing

| | |
|---|-----|
| FPGA-Based Real-Time Super-Resolution on an Adaptive Image Sensor | 125 |
| <i>Maria E. Angelopoulou, Christos-Savvas Bouganis, Peter Y.K. Cheung, and George A. Constantinides</i> | |
| A Parallel Hardware Architecture for Image Feature Detection | 137 |
| <i>Vanderlei Bonato, Eduardo Marques, and George A. Constantinides</i> | |
| Reconfigurable HW/SW Architecture of a Real-Time Driver Assistance System | 149 |
| <i>Josef Angermeier, Ulrich Batzer, Mateusz Majer, Jürgen Teich, Christopher Claus, and Walter Stechele</i> | |

Run-Time Behavior

| | |
|---|-----|
| A New Self-managing Hardware Design Approach for FPGA-Based Reconfigurable Systems | 160 |
| <i>S. Jovanović, C. Tanougast, and S. Weber</i> | |
| A Preemption Algorithm for a Multitasking Environment on Dynamically Reconfigurable Processor | 172 |
| <i>Vu Manh Tuan and Hideharu Amano</i> | |
| Accelerating Speculative Execution in High-Level Synthesis with Cancel Tokens | 185 |
| <i>Hagen Gädke and Andreas Koch</i> | |

Instruction Set Extension

| | |
|--|-----|
| ARISE Machines: Extending Processors with Hybrid Accelerators | 196 |
| <i>Nikolaos Vassiliadis, George Theodoridis, and Spiridon Nikolaidis</i> | |

| | |
|---|-----|
| The Instruction-Set Extension Problem: A Survey | 209 |
| <i>Carlo Galuzzi and Koen Bertels</i> | |

Random Number Generation and Financial Computation

| | |
|--|-----|
| An FPGA Run-Time Parameterisable Log-Normal Random Number Generator | 221 |
| <i>Pedro Echeverría, David B. Thomas, Marisa López-Vallejo, and Wayne Luk</i> | |
| Multivariate Gaussian Random Number Generator Targeting Specific Resource Utilization in an FPGA | 233 |
| <i>Chalermpol Saiprasert, Christos-Savvas Bouganis, and George A. Constantinides</i> | |
| Exploring Reconfigurable Architectures for Binomial-Tree Pricing Models | 245 |
| <i>Qiwei Jin, David B. Thomas, Wayne Luk, and Benjamin Cope</i> | |

Posters

| | |
|---|-----|
| Hybrid-Mode Floating-Point FPGA CORDIC Co-processor | 256 |
| <i>Jie Zhou, Yong Dou, Yuanwu Lei, and Yazhuo Dong</i> | |
| Multiplier-Based Double Precision Floating Point Divider According to the IEEE-754 Standard | 262 |
| <i>Vitor Silva, Rui Duarte, Mário Véstias, and Horácio Neto</i> | |
| Creating the World's Largest Reconfigurable Supercomputing System Based on the Scalable SGI® Altix® 4700 System Infrastructure and Benchmarking Life-Science Applications | 268 |
| <i>Haruna Cofer, Matthias Fouquet-Lapar, Timothy Gamerding, Christopher Lindahl, Bruce Losure, Alan Mayer, James Swoboda, and Teruo Utsumi</i> | |
| Highly Efficient Structure of 64-Bit Exponential Function Implemented in FPGAs | 274 |
| <i>Maciej Wielgosz, Ernest Jamro, and Kazimierz Wiatr</i> | |
| A Framework for the Automatic Generation of Instruction-Set Extensions for Reconfigurable Architectures | 280 |
| <i>Carlo Galuzzi and Koen Bertels</i> | |
| PARO: Synthesis of Hardware Accelerators for Multi-dimensional Dataflow-Intensive Applications | 287 |
| <i>Frank Hannig, Holger Ruckdeschel, Hritam Dutta, and Jürgen Teich</i> | |

| | |
|---|------------|
| Stream Transfer Balancing Scheme Utilizing Multi-path Routing in Networks on Chip | 294 |
| <i>Piotr Dziurzynski and Tomasz Maka</i> | |
| Efficiency of Dynamic Reconfigurable Datapath Extensions – A Case Study | 300 |
| <i>Steffen Köhler, Jan Schirok, Jens Braunes, and Rainer G. Spallek</i> | |
| Online Hardware Task Scheduling and Placement Algorithm on Partially Reconfigurable Devices | 306 |
| <i>Thomas Marconi, Yi Lu, Koen Bertels, and Georgi Gaydadjiev</i> | |
| Data Reallocation by Exploiting FPGA Configuration Mechanisms | 312 |
| <i>Oliver Sander, Lars Braun, Michael Hübner, and Jürgen Becker</i> | |
| A Networked, Lightweight and Partially Reconfigurable Platform | 318 |
| <i>Pierre Bomel, Guy Gogniat, and Jean-Philippe Diguet</i> | |
| Neuromolecularware – A Bio-inspired Evolvable Hardware and Its Application to Medical Diagnosis | 324 |
| <i>Yo-Hsien Lin and Jong-Chen Chen</i> | |
| An FPGA Configuration Scheme for Bitstream Protection | 330 |
| <i>Masaki Nakanishi</i> | |
| Lossless Compression for Space Imagery in a Dynamically Reconfigurable Architecture | 336 |
| <i>Xiaolin Chen, C. Nishan Canagarajah, Raffaele Vitulli, and Jose L. Nunez-Yanez</i> | |
| Author Index | 343 |