Lecture Notes in Computer Science 2799

Edited by G. Goos, J. Hartmanis, and J. van Leeuwen

Springer
Berlin
Heidelberg
New York
Hong Kong
London
Milan
Paris
Tokyo

Jorge Juan Chico Enrico Macii (Eds.)

Integrated Circuit and System Design

Power and Timing Modeling, Optimization and Simulation

13th International Workshop, PATMOS 2003
Turin, Italy, September 10-12, 2003
Proceedings

Springer

Volume Editors

Jorge Juan Chico
Universidad de Sevilla
Departamento de Tecnologia Electronica
Avenida Reina Mercedes, s/n., 41012 Sevilla, Spain
E-mail: jjchico@dte.us.es

Enrico Macii
Politecnico di Torino
Dipartimento di Automatica e Informatica
Corso Duca degli Abruzzi, 24,10129 Torino, Italy
E-mail: enrico.macii@polito.it

Cataloging-in-Publication Data applied for

A catalog record for this book is available from the Library of Congress

Bibliographic information published by Die Deutsche Bibliothek
Die Deutsche Bibliothek lists this publication in the Deutsche Nationalbibliografie; detailed bibliographic data is available in the Internet at <http://dnb.ddb.de>.

CR Subject Classification (1998): B.7, B.8, C.1, C.4, B.2, B.6, J.6

ISSN 0302-9743
ISBN 3-540-20074-6 Springer-Verlag Berlin Heidelberg New York

Springer-Verlag Berlin Heidelberg New York
a member of BertelsmannSpringer Science+Business Media GmbH

http://www.springer.de

Typesetting: Camera-ready by author, data conversion PTP-Berlin GmbH
Printed on acid-free paper SPIN 10931929 06/3142 5 4 3 2 1 0

Preface

Welcome to the proceedings of PATMOS 2003. This was the 13th in a series of international workshops held in several locations in Europe. Over the years, PATMOS has gained recognition as one of the major European events devoted to power and timing aspects of integrated circuit and system design. Despite its significant growth and development, PATMOS can still be considered as a very informal forum, featuring high-level scientific presentations together with open discussions and panel sessions in a free and relaxed environment.

This year, PATMOS took place in Turin, Italy, organized by the Politecnico di Torino, with technical co-sponsorship from the IEEE Circuits and Systems Society and the generous support of the European Commission, as well as that of several industrial sponsors, including BullDAST, Cadence, Mentor Graphics, STMicroelectronics, and Synopsys.

The objective of the PATMOS workshop is to provide a forum to discuss and investigate the emerging problems in methodologies and tools for the design of new generations of integrated circuits and systems. A major emphasis of the technical program is on speed and low-power aspects, with particular regard to modeling, characterization, design, and architectures.

A total of 85 contributed papers were received. Many thanks to all the authors that submitted their contributions. In spite of a very dense technical program, we were able to accept only 43 regular papers and 18 posters. Posters differ from regular papers in that they are presented to the audience during three sessions in which authors stand by cardboard displays and answer questions. Authors of regular papers, instead, deliver traditional oral presentations of their contributions during the sessions of the technical program.

Three keynote talks, offered by leading experts from industry and academia, served as starters for the three days of the workshop: Dr. Andrea Cuomo, Corporate VP of STMicroelectronics, Dr. Antun Domic, Senior VP of Synopsys Inc., and Dr. Ricardo Reis, Professor at the Universidad Federal Rio Grande do Sul addressed hot issues regarding architectures for next generation integrated platforms, EDA tools for energy-efficient design, and physical synthesis for high-speed and low-power circuits, respectively.

An industrial session, in which scientists from EDA and IC manufacturing companies illustrated their most recent advances in R&D activities and leading-edge technology development complemented the technical program.

Finally, a one-hour panel session took advantage of the presence of Officers from the European Commission and Coordinators of large EU-funded collaborative projects to provide insights into the new instruments and mechanisms now available in Europe for supporting research and innovation activities.

Last, but not least, a rich social program, paired with an industrial exhibition, guaranteed additional opportunities for establishing new relationships among the workshop participants.

Many thanks to the technical program committee for all their hard work in paper review, paper selection, and session organization. Additional experts also collaborated in the review process, and we acknowledge their contribution. Lists of technical program committee members and of additional reviewers can be found the following pages. Thanks also to the invited speakers for graciously donating their time and to the panelists for an enlightening and entertaining session.
We hope you found the workshop both stimulating and helpful and that you will enjoyed your stay in Turin for the whole duration of the event.

September 2003

Jorge Juan Chico
Enrico Macii

Organization

Organizing Committee

General Chair:	Prof. Enrico Macii, Politecnico di Torino, Italy
Program Chair:	Prof. Jorge Juan Chico, Universidad de Sevilla, Spain
Industrial Chair:	Dr. Roberto Zafalon, STMicroelectronics, Italy
Conference Manager:	Ms. Agnieszka Furman, Politecnico di Torino, Italy

Program Committee

D. Auvergne, U. Montpellier, France
J. Bormans, IMEC, Belgium
J. Figueras, U. Catalunya, Spain
J. A. Carballo, IBM, USA
C. E. Goutis, U. Patras, Greece
A. Guyot, INPG Grenoble, France
R. Hartenstein, U. Kaiserslautern, Germany
S. Jones, U. Loughborough, UK
P. Larsson-Edefors, Chalmers T.U. Sweden
V. Moshnyaga, U. Fukuoka, Japan
W. Nebel, U. Oldenburg, Germany
J.A. Nossek, T.U. Munich, Germany
A. Nunez, Las Palmas, Spain
M. Papaefthymiou, U. Michigan, USA
F. Pessolano, Philips, The Netherlands
H. Pfleiderer, U. Ulm, Germany
C. Piguet, CSEM, Switzerland
R. Reis, U. Porto Alegre, Brazil
M. Robert, U. Montpellier, France
A. Rubio, U. Catalunya, Spain
D. Sciuto, Politecnico di Milano, Italy
D. Soudris, U. Trace, Greece
J. Sparsø, DTU, Denmark
A. Stauffer, EPFL, Switzerland
A. Stempkowsky, Acad. of Sciences, Russia
T. Stouraitis, U. Patras, Greece
A.M. Trullemans-Anckaert, U. Louvain-la-Neuve, Belgium
R. Zafalon, STMicroelectronics, Italy

PATMOS Steering Committee

D. Auvergne, U. Montpellier, France
R. Hartenstein, U. Kaiserslautern, Germany
W. Nebel, U. Oldenburg, Germany
C. Piguet, CSEM, Switzerland
A. Rubio, U. Catalunya, Spain
J. Figueras, U. Catalunya, Spain
B. Ricco, U. Bologna, Italy
D. Soudris, U. Trace, Greece
J. Sparsø, T.U. Denmark
A.M. Trullemans-Anckaert, U. Louvain, Belgium
P. Pirsch, U. Hannover, Germany
B. Hochet, EIVd, Switzerland
A.J. Acosta, U. Sevilla/IMSE-CNM, Spain
J. Juan, U. Sevilla/IMSE-CNM, Spain
E. Macii, Politecnico di Torino, Italy
R. Zafalon, STMicroelectronics, Italy
V. Paliouras, U. Patras, Greece
J. Vounckx , IMEC, Belgium

Executive Sub-committee

President:	Joan Figueras, U. Catalunya, Spain
Vice-president:	Reiner Hartenstein, U. Kaiserslautern, Germany
Secretary:	Wolfgang Nebel, U. Oldenburg, Germany

Reviewers

A. Acosta
D. Auvergne
N. Azemard
P. Babighian
M.J. Bellido
L. Bisdounis
A. Bona
J.A. Carballo
J.M. Daga
A. Dehnhardt
M. Donno
J. Figueras
L. Friebe
F. Fummi
C. Goutis
J. Luis Güntzel
A. Guyot
E. Hall
K. Inoue
A. Ivaldi
J. Jachalsky
R. Jiménez
J. Juan
K. Karagianni
C. Kashyap
H. Klussman
O. Koufopavlou
S. Lagudu
C. Lefurgy
J.D. Legat
J. Van Lunteren
A. Macii
S. Manich
K. Masselos
P. Maurine
M. Meijer
S. Moch
V. Moshnyaga
W. Nebel
S. Nikolaidis
N. Nolte
A. Nuñez
M. Papaefthymiou
F. Pessolano
H.-J. Pfleiderer

C. Piguet
P. Pirsch
C. Psychalinos
R. Reis
J. Rius
F. Salice
A. Schallenberg
D. Sciuto
H. Shafi
C. Silvano
C. Simon-Klar
D. Soudris
J. Sparsø
A. Stempkowsky
G. Theodoridis
A. Tisserand
L. Torres
A.M. Trullemans
M. Valencia
S.-M. Yoo
V. Zaccaria
R. Zafalon
M. Wahle
M. Winter

Sponsors and Industrial Supporters

IEEE Circuits and Systems Society (Technical Co-sponsor)
Politecnico di Torino
European Commission
BullDAST s.r.l.
Cadence Design Systems, Inc.
Mentor Graphics, Italian Site
STMicroelectronics, s.r.l.
Synopsys, Inc.

Table of Contents

Keynote Speech

Gate-Level Modeling and Design

Low Level Modeling and Characterization

Interconnect Modeling and Optimization

Asynchronous Techniques

Keynote Speech

Industrial Session

RTL Power Modeling and Memory Optimisation

High-Level Modeling

Power Efficient Technologies and Designs

Keynote Speech

Communication Modeling and Design

Low Power Issues in Processors and Multimedia

Poster Session 1

Poster Session 2

Poster Session 3