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Power - Aware Computer Systems

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Preface

Welcome to the proceedings of the 3rd Power-Aware Computer Systems (PACS 2003) Workshop held in conjunction with the 36th Annual International Symposium on Microarchitecture (MICRO-36). The increase in power and energy dissipation in computer systems has begun to limit performance and has also resulted in higher cost and lower reliability. The increase also implies reduced battery life in portable systems. Because of the magnitude of the problem, all levels of computer systems, including circuits, architectures, and software, are being employed to address power and energy issues. PACS 2003 was the third workshop in its series to explore power- and energy-awareness at all levels of computer systems and brought together experts from academia and industry.

These proceedings include 14 research papers, selected from 43 submissions, spanning a wide spectrum of areas in power-aware systems. We have grouped the papers into the following categories: (1) compilers, (2) embedded systems, (3) microarchitectures, and (4) cache and memory systems.

The first paper on compiler techniques proposes pointer reuse analysis that is biased by runtime information (i.e., the targets of pointers are determined based on the likelihood of their occurrence at runtime) to map accesses to energy-efficient memory access paths (e.g., avoid tag match). Another paper proposes compiling multiple programs together so that disk accesses across the programs can be synchronized to achieve longer sleep times in disks than if the programs are optimized separately.

The first paper on embedded systems proposes scaling down the components (display, wireless, and CPU) of a mobile system to match user requirements while reducing energy. The second paper explores an integer linear programming approach for embedded systems to decide which instructions should be held in a low-power scratchpad instead of a high-power instruction cache. The next paper predicts battery life at runtime to help the operating system in managing power. The next paper proposes a tiled architecture that exploits parallelism enabled by global interconnects and synchronized design to achieve high energy efficiency. The last paper in this group proposes a policy to decide which of the multiple wireless network interfaces provided in a mobile device should be used based on the power and performance needs of the mobile system.

The third group of papers focuses on microarchitecture techniques, and includes an analysis of energy, area, and speed trade-offs between table lookup for instruction reuse and actual computation. Another paper proposes scheduling transactions in a multiprocessor to as few CPUs as possible to increase the number of CPUs in deep-sleep state. The next paper evaluates the extent of energy savings achieved by avoiding instructions that are either not needed for correct behavior or not committed, and by sizing microarchitectural structures. The last paper proposes coupled power and thermal simulation and studies the effect of temperature on leakage energy.

The last group proposes techniques to reduce power in caches and memory. The first paper in this group studies the interaction between dynamic voltage scaling (DVS) and power-aware memories and proposes policies to control the CPU's DVS setting and the memory's power setting together. The next paper uses the criticality of instructions to determine which locations should be placed in high-speed cache banks and which in low-power banks. The last paper proposes applying high-performance techniques only to the most-frequently-used instruction traces and saving power on the other traces.

PACS 2003 was successful due to the quality of the submissions, the efforts of the program committee, and the attendees. We would like to thank Pradip Bose for his interesting keynote address, which described microarchitectural choices at the early architecture-definition stage to achieve power and energy efficiency. We would like to also thank Glen Reinman, Jason Fritts, and the other members of the MICRO-36 organizing committee who helped arrange the local accommodations and publicize the workshop.

December 2003   Babak Falsafi and T.N. Vijaykumar

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