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Ricardo Póvoa
To my dear Marta, for everything that is worth fighting for.

João Goes
To Valentim and Madalena.

Nuno Horta
To Carla, João, and Tiago.

Preface

Amplifiers are important in several electronic systems and processing chains, e.g., radio-frequency transceivers in wireless networks, data acquisition channels, or analog-to-digital converters (ADCs). Therefore, the applications of amplifiers spread from analog to mixed-signal design. Desirably, amplifiers allow an efficient amplification of small-signals, without adding significant noise to the chain, and can also operate as signal comparators in ADCs. The power reduction necessity, the intrinsic gain reduction and high variability, with the low-supply voltage trend of modern CMOS technologies, has driven the evermore challenging design of amplifiers to implement multiple gain stages and possibly one output driver stage. Regarding single-stage amplifiers, commonly more power efficient, high gains are normally achieved using cascode devices or cascaded stages. However, this leads to reduced output swings (OS) due to the lower supply voltages in hand with the stacking of devices. In residue amplifiers, inside ADCs, one possible solution is dynamic amplification. Dynamic CMOS amplifiers are proposed by Copeland and Rabaey, in 1979, in which the idea is that the bias current is not constant but changed during amplification. This property is important, particularly in switched-capacitor circuits, where the amplifier can be biased in strong inversion with a large current in the beginning and then continuously reduced the current toward weak inversion, until the power is practically cut off, maximizing both the gain and the OS of the amplifier. This work addresses the need for energy-efficient amplifiers and gain enhancement strategies, compatible with lower supply voltages, by proposing a complete new family of single-stage cascode-free amplifiers, with design, optimization, and experimental evaluation. The energy efficiency and topological potential are maximized through advanced automation carried by AIDA, an analog IC design and optimization framework, based on computational intelligence. The topologies are proposed using the UMC 130 nm CMOS technology for proof of concept: voltage combiners (VC) biased operational transconductance amplifier (OTA), VC biased OTA with current starving for higher gain and energy efficiency, folded VC biased OTA for lower-voltage sources, and a dynamic VC biased OTA targeting ADCs, with gains above 50 dB and energy-efficient figure-of-merit values of 1024,

1102, 2279, and 1349 MHz × pF/mA, correspondingly. The presented results are beyond what is achievable with a classic folded-cascode amplifier, and, regarding dynamic amplifiers, the proposed solutions clearly contribute to advances in the state of the art. This work is organized in six chapters. Chapter 1 presents a brief introduction with the motivation and context to develop and propose new amplifier topologies, with high energy efficiency and gain improvement, particularly in the environment of the Internet of Things, emphasizing the wide field of applications of amplifiers. Chapter 2 discusses the background and the state of the art of single-stage amplifiers, providing the context of the developed work. The main topologies are detailed: the telescopic-cascode, the mirrored-cascode, and the folded-cascode amplifiers, followed by the recycling folded-cascode amplifier with the corresponding improvements and surveying the concept of dynamic amplification in CMOS technologies. The performance metrics are summarized, and a throughout comparison of the prior art is provided. Chapter 3 presents the architectures proposed in this work and shows circuit implementations in detail. The basic voltage-combiner structure is presented and detailed both at analytical and simulation levels. The complete set of amplifiers is shown, both in terms of topological description and analytic analysis. Sizing strategies and initial designs, i.e., first approaches that guarantee functional circuits, are presented with results at simulation level, validating the proposed topologies with applied noise modeling. Chapter 4 presents the optimization framework, AIDA; the complete setup for the optimization, regarding the objectives, specifications, variables, and ranges; and post-optimization simulation results for selected sizing solutions, positioning the proposed circuits in the context of the state of the art of single-stage amplifiers. Chapter 5 presents the printed circuit board developed to properly measure the fabricated circuits during the course of the present dissertation. The prototyped solutions are detailed: layout, post-layout, Monte Carlo simulations, experimental measurements, and comparison with the state of the art. Finally, Chapter 6 draws the conclusions, compounded with a summary of all the achieved developments, positioning the proposed topologies relative to the state of the art of single-stage amplification architectures.

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Contents

List of Abbreviations

AA	Active area
AC	Alternate current
ADC	Analog-to-digital converter
AIDA	Analog Integrated Circuit Design Automation
AMG	Analog module generator
CD	Common-drain
CG	Common gate
CMFB	Common-mode feedback
CMOS	Complementary metal-oxide-semiconductor
CMRR	Common-mode rejection ratio
CNT	Carbon nanotube
COB	Chip-on-board
CPU	Central processing unit
CS	Common source
DC	Direct current
DEL	Saturation margin
DFT	Discrete Fourier transform
ESD	Electrostatic discharge
FCA	Folded-cascode amplifier
FF	Fast NMOS and fast PMOS
FFT	Fast Fourier transform
FNSP	Fast NMOS and slow PMOS
FOM	Figure of merit
GBW	Gain-bandwidth product
GDS	Geometric data stream
HVHT	High voltage high temperature
HVLT	High voltage low temperature
IC	Integrated circuits
IOT	Internet of Things

LVHT	Low voltage high temperature
LVLT	Low voltage low temperature
MC	Monte Carlo
MCA	Mirrored-cascode amplifier
MOSFET	Metal-oxide-semiconductor field-effect transistor
NMOS	n-channel MOSFET
NSGA	Non-sorting genetic algorithm
OPAMP	Operational amplifier
OPDK	Organic process design kit
OS	Output swing
OTA	Operational transconductance amplifier
OTFT	Organic thin-film transistor
OVD	Overdrive voltage
PCB	Printed circuit board
PM	Phase margin
PMOS	p-channel MOSFET
POF	Pareto optimal front
PSRR	Power-supply rejection ratio
PVT	Process, voltage, and temperature
RAM	Random-access memory
RF	Radio-frequency
RFCA	Recycling folded-cascode amplifier
RFID	Radio-frequency identification
RMS	Root mean square
SAR	Successive approximation register
SC	Switched-capacitor
SMA	Surface Mount Adhesive
SMD	Surface Mount Device
SNFP	Slow NMOS and fast PMOS
SOIC	Small Outline Integrated Circuit
SR	Slew rate
SS	Slow NMOS and slow PMOS
S/H	Sample-and-hold
TCA	Telescopic-cascode amplifier
TF	Transfer function
VC	Voltage combiner
VOS	Offset voltage
VT	Threshold voltage
UMC	United Microelectronics Corporation
WF	Width-*per*-finger

List of Symbols

a_v	Voltage gain
a_{cm}	Common-mode voltage gain
a_{dm}	Differential-mode voltage gain
b	Mirroring factor
c	Light speed in vacuum
c_{db}	Small-signal drain-bulk capacitance
c_{gd}	Small-signal gate-drain capacitance
c_{gs}	Small-signal gate-source capacitance
c_l	Load capacitance
c_{ox}	Gate oxide capacitance *per* unit of area
c_s	Sampling capacitance
cmfb	Common-mode feedback
f	Frequency
$f_{-3\ db}$	Bandwidth
f_c	Corner frequency
f_m	Objective function
g_m	Constraints function
gds	Small-signal drain-source conductance
gm	Small-signal transconductance
i	Electric current
i_d	Drain current
i_{dd}	Current consumption
i_{dsat}	Saturation current
i_o	Output current
i_{ref}	Reference current
k	Boltzmann constant
l	Channel length
nf	Channel number of fingers
p_m	Performance figures
q	Electric charge

r_{eq}	Equivalent resistance
r_o	Output resistance
t	Time unit
t_{ox}	Gate oxide thickness
v_{bias}	Bias voltage
v_{cm}	Common-mode voltage
v_d	Differential-mode voltage
v_{dd}	Positive supply voltage
v_{ds}	Drain-source voltage
vds_{sat}	Saturation voltage
v_{gs}	Gate-source voltage
v_i	Input voltage
v_o	Output voltage
v_{reg}	Voltage regulator output voltage
v_{ss}	Negative supply voltage
v_t	Threshold voltage
w	Channel width
y	Admittance
ε	Epsilon
ε_{ox}	Oxide permittivity
κ	Velocity-saturation degree
λ	Wavelength
μ	Channel mobility
ξ_c	Velocity-saturation threshold
σ	Sigma
ω_p	Pole frequency