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Kamran Souri • Kofi A.A. Makinwa

Energy-Efficient Smart Temperature Sensors in CMOS Technology

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Mountain View, CA, USA Kamran Souri
May 2017

Contents

About the Authors

Kamran Souri was born in Tabriz, Iran, in 1980. He received his B.Sc. in Electronics and M.Sc. in Telecommunication Systems from Amirkabir University of Technology, Iran, in 2001 and 2004, respectively. In Sept. 2007, he joined the Electronic Instrumentation Laboratory (EI-Lab), TU-Delft, where he received his M.Sc. degree (cum laude) in Micro-electronics in 2009 and Ph.D. degree in 2016 for his research on energy-efficient smart temperature sensors in CMOS technology.

From 2001 to 2007, he worked at PSP-Ltd, Tehran, Iran, designing embedded systems for use in high-quality audio/video systems and KVM switches. From 2008 to 2009, he was an intern at NXP Semiconductors, Eindhoven, designing energy-efficient temperature sensors for use in RFID tags. Since 2014, he has been with SiTime Corp., Santa Clara, United States, where he is currently a Principal Circuit Design Engineer, focusing on the design of MEMS-based oscillators.

Dr. Souri was the recipient of the IEEE Solid-State Circuits Society Predoctoral Achievement Award in 2013. He has also served as the technical reviewer for several journals in the field, among them the *IEEE Journal of Solid-State Circuits* (JSSC), *Analog Integrated Circuits and Signal Processing* (AICSP), and the *IEEE Transactions on Circuits and Systems* (TCAS).

Kofi A.A. Makinwa received his B.Sc. and M.Sc. degrees from Obafemi Awolowo University, Nigeria, in 1985 and 1988, respectively. In 1989, he received an M.E.E. degree from the Philips International Institute, the Netherlands, and in 2004, a Ph.D. degree from Delft University of Technology, the Netherlands.

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Kofi Makinwa is the Analog Subcommittee Chair of the International Solid-State Circuits Conference (ISSCC). He is also on the program committees of the VLSI Symposium, the European Solid-State Circuits Conference (ESSCIRC), and the Advances in Analog Circuit Design (AACD) workshop. He has been a guest editor of the *Journal of Solid-State Circuits* (JSSC) and a distinguished lecturer of the IEEE Solid-State Circuits Society. For his doctoral research, he was awarded the 2005 Simon Stevin Gezel Award from the Dutch Technology Foundation. He is a co-recipient of 14 best paper awards, from the JSSC, ISSCC, VLSI, and Transducers, among others. At the 60th anniversary of ISSCC he was recognized as a top-10 contributor. He is an IEEE Fellow, an alumnus of the Young Academy of the Royal Netherlands Academy of Arts and Sciences, and an elected member of the IEEE Solid-State Circuits Society AdCom, the society's governing board.

Summary

Nowadays, smart temperature sensors, i.e., sensors with digital outputs, are widely used in various systems. Integrating smart sensors into wireless systems such as RFID tags or wireless sensor networks (WSNs) enables wireless temperature sensing, which in turn opens up a wide range of new applications. This thesis describes the requirements, design, and implementation of smart temperature sensors for use in wireless temperature sensing.

In Chap. 1, an introduction to wireless temperature sensing and its requirements is given. Typically, a wireless node is either powered by a battery or scavenges its energy from the environment, e.g., from an external RF magnetic field. Due to the limited amount of energy available, energy efficiency of the integrated sensor restricts either the battery's lifetime or the operating range of the wireless node. On the other hand, mass production imposes stringent requirements on the cost, which calls for CMOS-compatible sensors. To obtain sufficient accuracy, however, CMOS sensors often require time-consuming (and thus costly) *calibration*: a process in which the sensor's output is compared with that of a reference sensor at a number of known temperatures. The information obtained during calibration is then used to *trim* the sensor, thereby improving its accuracy. A short survey of various CMOS compatible choices is presented. It is shown that substrate PNPs are suitable candidates for wireless temperature sensing. They are power-efficient and exhibit a well-defined process spread, which can be effectively trimmed at a single temperature. However, they require supply voltages greater than $\approx 1.2\,\text{V}$, making them ill suited for low-voltage applications and nano-scale CMOS processes. A promising alternative is to bias a MOSFET in the subthreshold region, while its body and gate terminals are shorted. This so-called DTMOST configuration enables sub-1V operation while exhibiting less spread when compared to the bulk configuration. Finally, to facilitate the comparison between energy efficiency of various temperature sensors, a single figure of merit (FoM) is presented.

In Chap. 2, the operating principle of BJT-based smart temperature sensors is presented. Using the parasitic BJTs available in CMOS, a complementary-to-absolute-temperature (CTAT) voltage V_{BE} and a proportional-to-absolute-temperature (PTAT) voltage ΔV_{BE} can be generated. By properly scaling ΔV_{BE}

(with a scalar α) and combining it with V_{BE}, a reference voltage V_{REF} can then be obtained. In a generic BJT readout, the ratio of $\alpha \cdot \Delta V_{\mathrm{BE}}$ and V_{REF} is digitized by means of an analog-to-digital converter (ADC) to generate a PTAT ratio μ. The resolution requirement of the ADC is also discussed. It is shown that almost $\frac{2}{3}$ of the ADS's dynamic range is wasted with this approach. To identify the energy efficiency of existing sensors prior to the start of this research, a study of energy efficiency limits in BJT-based sensors is presented. In this analysis, the ultimate energy efficiency of a BJT-based sensor front-end is calculated and the theoretical limits are defined. Two different approaches based on bias-current and emitter-area scaling are considered. Based on this analysis, a significant energy-efficiency gap, over four orders of magnitude, is observed between the prior-art and theoretical limits. The study of various sensor architectures reveals that, in fact, the reason behind this gap lies in the employed readout circuits, which mostly include $\Delta\Sigma$- or SAR-ADCs. They either suffer from long conversion times and poor power efficiency, or are not capable of providing the target resolution or accuracy. To bridge this efficiency gap, a new readout architecture is clearly required.

In Chap. 3, different BJT-based sensor architectures based on digitizing nonlinear ratios between ΔV_{BE} and V_{BE} (or their combinations) are explored. The required linearization to calculate the PTAT ratio μ is then performed in the digital back-end. Since the coefficient α is digitally implemented, it can also be used for trimming. The employed ADC architectures in these examples, however, often result in more waste of dynamic range than in the generic approach, exacerbating the lack of energy efficiency. To address this issue, a new readout topology based on digitizing the ratio $X = V_{\mathrm{BE}}/\Delta V_{\mathrm{BE}}$ is proposed. Since temperature changes are rather slow, the ratio X is accurately digitized by a two-step *zoom*-ADC. As X is typically greater than one, it can be expressed as $X = n + \mu'$, where n and μ' correspond to the integer and fractional parts, respectively. First, a full-range SAR conversion obtains the integer n by performing a binary search algorithm, comparing V_{BE} to integer multiples of ΔV_{BE}. This is then followed by a low-range fine $\Delta\Sigma$ converter, whose references are set to n and $n + 1$. In this manner, the ratio μ' can be accurately digitized with high resolution. In contrast to the conventional $\Delta\Sigma$-ADCs, the full-scale range of the fine converter in the zoom-ADC is considerably reduced, which notably relaxes various key requirements such as the number of $\Delta\Sigma$-cycles and the DC gain and swing of the loop filter. In this architecture, both conversion time and power efficiency can be improved, which results in a substantial improvement in energy efficiency. The fact that dynamic correction techniques can be used in the fine conversion phase ensures that the accuracy of the zoom-ADC can be as good as that of conventional $\Delta\Sigma$-ADC architectures.

In Chap. 4, a low-power BJT-based sensor prototype based on a 1st-order switched-capacitor (SC) zoom-ADC is presented. It achieves a resolution of 15 mK in a conversion time of 100 ms while dissipating only 4.6 μA. After a single α-trim at 25 °C, the sensor obtains an inaccuracy of ± 0.2 °C (3σ) from -30 to 125 °C. This result shows 11× energy efficiency improvement when compared to sensors with similar accuracy, back in 2011. However, its fine conversion step employs a slow, 1st-order $\Delta\Sigma$ modulator, limiting its energy efficiency. Moreover, each

$\Delta\Sigma$ cycle requires two full clock periods, since V_{BE} and ΔV_{BE} are separately sampled/integrated. To further improve the sensor's energy efficiency, a second prototype is realized which achieves similar resolution in about 16× less conversion time, while drawing 25% less supply current. This is achieved by using a 2nd-order zoom-ADC, combined with a new charge-balancing scheme, whose operation is based on *simultaneous* sampling of V_{BE} and ΔV_{BE}. This allows the use of low-swing, low-power amplifiers. The sensor's energy efficiency is therefore improved by over 20× compared to the first prototype. Using a thermal calibration and digital PTAT trimming at 30 °C, the sensor achieves an inaccuracy of ±0.15 °C (3σ) from −55 to 125 °C. Moreover, a voltage calibration technique based on electrical measurements is also explored, which is significantly faster (only requires 200 ms), while achieving comparable accuracy. The impact of batch-to-batch spread and plastic packaging on sensor's accuracy is investigated as well. As observed, both of them can cause temperature reading shifts in the order of 0.4–0.5 °C from −55 to 125 °C.

In the last part of Chap. 4, a BJT-based sensor prototype for sensing high temperatures (>150 °C) is also demonstrated. It is shown that by optimizing the emitter area and bias current of a substrate PNP, the impact of saturation current I_S at high temperatures can be mitigated. Furthermore, robust circuit techniques are employed to cope with the various leakage currents at such temperatures, which would otherwise impact the accuracy of V_{BE} and ΔV_{BE}, and thus the sensor output. It achieves an inaccuracy of ±0.4 °C (3σ) from −55 to 200 °C, which is similar to that of state-of-the-art sensors capable of operating over such temperature ranges. However, it draws only 22 µA, which is more than an order of magnitude less.

In Chap. 5, the use of DTMOSTs as temperature sensing elements is demonstrated. When operated in weak inversion, the gate-source voltage V_{GS} of a DTMOST is almost half of the base-emitter voltage V_{BE}, thus enabling sub-1V operations. Moreover, compared to a diode-connected MOSFET, the V_{GS}–I_D characteristic of a diode-connected DTMOST is less sensitive to the spread in threshold voltage V_T, making it a promising candidate for realizing accurate temperature sensors. Two sensor prototypes based on such sensing elements are demonstrated in a chosen 160 nm CMOS process. After a single-temperature trim, the first prototype achieves an inaccuracy of ±0.4 °C (3σ) from −55 to 125 °C, and enables an apples-to-apples comparison with BJTs, proving that DTMOSTs are indeed only a factor 2× less accurate. In the second prototype, the low-voltage capability of DTMOSTs is then exploited to realize a sub-1V, sub-µW precision sensor. Employing fully inverter-based SC integrators, a 2nd-order zoom-ADC is realized in the second prototype. It can operate at supply voltages as low as 0.85 V, while drawing only 700 nA. It also maintains the same inaccuracy of ±0.4 °C (3σ) from −40 to 125 °C, after a single-temperature trim. These results prove that DTMOSTs could be considered as the temperature sensors of choice when sub-1V, high accuracy, and energy efficiency are key requirements.

In Chap. 6, the main findings of this work are summarized. These include the development of the zoom-ADC and its application in energy-efficient smart temperature sensors. The final prototype BJT-based sensor achieved a resolution

FoM of 11 pJ °C^2 and improved state of the art by a factor of 15× (in 2012). Another key finding was the fact that DTMOST sensors enable low-voltage operations while being only 2× less accurate than BJT-based sensors. The final prototype achieved a fairly good energy efficiency, evidenced by a FoM of 14 pJ °C^2. The chapter also contains some suggestions for future work: to further improve the energy efficiency, continuous-time (CT) readouts could be considered as promising alternatives to the switched-capacitor circuits. Furthermore, to reduce the cost of over-temperature characterizations, a combination of voltage calibration with integrated heaters could be used to quickly extract the global calibration parameters. Another alternative could be to exploit the high accuracy of thermal-diffusivity (TD) sensors as on-die references during the calibration process. The chapter ends with a discussion of the potential use of the zoom-ADC technique to realize general-purpose ADCs with high energy efficiency.