Testing of Interposer-Based 2.5D Integrated Circuits

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To my parents,
Xuechen Wang and Yulan Shi for their endless support.
To my love
Xiaowen Han for her dedication and accompany!

– Ran Wang

Preface

The unprecedented and relentless growth in the electronics industry is feeding the demand for integrated circuits (ICs) with increasing functionality and performance at minimum cost and power consumption. As predicted by Moore's law, ICs are being aggressively scaled to meet this demand. While the continuous scaling of process technology is reducing gate delays, the performance of ICs is being increasingly dominated by interconnect delays. In an effort to improve submicrometer interconnect performance, to increase packing density, and to reduce chip area and power consumption, the semiconductor industry is focusing on three-dimensional (3D) integration. However, volume production and commercial exploitation of 3D integration are not feasible yet due to significant technical hurdles.

At the present time, interposer-based 2.5D integration is emerging as a precursor to stacked 3D integration. All the dies and the interposer in a 2.5D IC must be adequately tested for product qualification. However, since the structure of 2.5D ICs is different from the traditional 2D ICs, new challenges have emerged: (1) pre-bond interposer testing, (2) lack of test access, (3) limited ability for at-speed testing, (4) high-density I/O ports and interconnects, (5) reduced number of test pins, and (6) high power consumption. This research targets that the above challenges and effective solutions have been developed to test both dies and the interposer.

The book first introduces the basic concepts of 3D ICs and 2.5D ICs. Prior work on testing of 2.5D ICs is studied. An efficient method is presented to locate defects in a passive interposer before stacking. The proposed test architecture uses e-fuses that can be programmed to connect or disconnect functional paths inside the interposer. The concept of a die footprint is utilized for interconnect testing, and the overall assembly and test flow is described. Moreover, the concept of weighted critical area is defined and utilized to reduce test time. In order to fully determine the location of each e-fuse and the order of functional interconnects in a test path, we also present a test-path design algorithm. The proposed algorithm can generate all test paths for interconnect testing.

In order to test for opens, shorts, and interconnect delay defects in the interposer, a test architecture is proposed that is fully compatible with the IEEE 1149.1

standard and relies on an enhancement of the standard test access port (TAP) controller. To reduce test cost, a test-path design and scheduling technique is also presented that minimizes a composite cost function based on test time and the design-for-test (DfT) overhead in terms of additional through silicon vias (TSVs) and micro-bumps needed for test access. The locations of the dies on the interposer are taken into consideration in order to determine the order of dies in a test path.

To address the scenario of high density of I/O ports and interconnects, an efficient built-in self-test (BIST) technique is presented that targets the dies and the interposer interconnects. The proposed BIST architecture can be enabled by the standard TAP controller in the IEEE 1149.1 standard. The area overhead introduced by this BIST architecture is negligible; it includes two simple BIST controllers, a linear-feedback shift register (LFSR), a multiple-input signature register (MISR), and some extensions to the boundary-scan cells in the dies on the interposer. With these extensions, all boundary-scan cells can be used for self-configuration and self-diagnosis during interconnect testing. To reduce the overall test cost, a test scheduling and optimization technique under power constraints is described.

In order to accomplish testing with a small number test pins, the book presents two efficient ExTest scheduling strategies that implements interconnect testing between tiles inside an system on chip (SoC) die on the interposer while satisfying the practical constraint that the number of required test pins cannot exceed the number of available pins at the chip level. The tiles in the SoC are divided into groups based on the manner in which they are interconnected. In order to minimize the test time, two optimization solutions are introduced. The first solution minimizes the number of input test pins, and the second solution minimizes the number of output test pins. In addition, two subgroup configuration methods are further proposed to generate subgroups inside each test group.

Finally, the book presents a programmable method for shift-clock stagger assignment to reduce power supply noise during SoC die testing in 2.5D ICs. An SoC die in the 2.5D IC is typically composed of several blocks and two neighboring blocks that share the same power rails should not be toggled at the same time during shift. Therefore, the proposed programmable method does not assign the same stagger value to neighboring blocks. The positions of all blocks are first analyzed, and the shared boundary length between blocks is then calculated. Based on the position relationships between the blocks, a mathematical model is presented to derive optimal result for small-to-medium-sized problems. For larger designs, a heuristic algorithm is proposed and evaluated.

In summary, this book targets important design and optimization problems related to testing of interposer-based 2.5D ICs. The research reported in the book has led to theoretical insights, experiment results, and a set of test and design-for-test methods to make testing effective and feasible from a cost perspective.

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Contents

1 Introduction 1
1.1 The Evolution of 2.5D ICs 1
1.1.1 3D ICs: A Paradigm Shift from Traditional Integrated Circuits 1
1.1.2 2.5D ICs: An Alternative to 3D ICs 2
1.2 Research Challenges and Motivation 4
1.2.1 Pre-bond Interposer Testing 4
1.2.2 Lack of Test Access 5
1.2.3 Limited Ability for At-Speed Testing 5
1.2.4 High-Density I/O Ports and Interconnects 6
1.2.5 Reduced Number of Test Pins 6
1.2.6 High Power Consumption 6
1.3 Emerging Solutions for the Testing of 2.5D ICs 7
1.4 Outline of the Book 12
References 14

2 Pre-bond Testing of the Silicon Interposer 17
2.1 Background 18
2.2 Proposed Test Architecture and Procedures 19
2.2.1 Definition of Die Footprint 19
2.2.2 Test Architecture 20
2.2.3 Assembly and Test Flow 23
2.2.4 Test Procedures 24
2.2.5 Weighted Critical Area 27
2.3 Test-Path Design 28
2.3.1 Optimization Problem 28
2.3.2 Proposed Algorithm 32
2.4 Experimental Results 37
2.4.1 Testing the Horizontal Interconnects 37

2.4.2 Testing for Vertical Interconnects . . . 39
2.4.3 Evaluation of the Test-Path Design Method . . . 41
2.5 Conclusion . . . 47
References . . . 47

3 Post-bond Scan-Based Testing of Interposer Interconnects . . . 49
3.1 Problem Statement . . . 50
3.2 Proposed Test Architecture . . . 51
3.3 Test Application . . . 53
3.3.1 Open/Short-Defect Testing . . . 54
3.3.2 Delay-Defect Testing . . . 54
3.3.3 Test Structures for Bi-directional I/Os . . . 58
3.4 Integration with IEEE 1149.1 . . . 60
3.5 Simulation Results . . . 66
3.5.1 Detection Capability for Open Defects . . . 66
3.5.2 Detection Capability for Short Defects . . . 69
3.5.3 Detection Capability for Delay Defects . . . 70
3.5.4 Architecture Simulation . . . 75
3.5.5 Area Overhead . . . 78
3.6 Conclusion . . . 79
References . . . 79

4 Test Architecture and Test-Path Scheduling . . . 81
4.1 Proposed Test Architecture . . . 82
4.1.1 Boundary-Scan Structure . . . 82
4.1.2 Modified TAP Controller . . . 83
4.1.3 Boundary-Scan Cells and Circuit Block . . . 85
4.1.4 Test Procedures . . . 88
4.2 Test-Path Design and Scheduling . . . 89
4.2.1 Structure of Additional Test Paths . . . 91
4.2.2 Minimization of Total Interconnect Test Cost . . . 92
4.2.3 Optimization in Alternative Scenarios . . . 94
4.2.4 Placement of Dies on the Test Path . . . 95
4.3 Simulation Results . . . 98
4.3.1 Test Architecture Simulation Results . . . 98
4.3.2 Case Study . . . 100
4.3.3 Area Overhead . . . 101
4.3.4 Test-Path Design and Scheduling Results . . . 102
4.4 Conclusion . . . 107
References . . . 107

5 Built-In Self-Test . . . 109
5.1 Related Prior Work . . . 110
5.2 Proposed BIST Architecture . . . 110

5.3 BIST Components 113
5.3.1 Self-configuration of the In-BSC 113
5.3.2 Pattern Generator 114
5.3.3 Response Compactor 117
5.3.4 BIST Controller 119
5.4 Test Scheduling and Optimization 121
5.5 Simulation Results 125
5.5.1 BIST Architecture Simulation 125
5.5.2 Case Study 126
5.5.3 Overhead Analysis 128
5.5.4 Test Scheduling Results 129
5.6 Conclusion 132
References 132

6 ExTest Scheduling and Optimization 135
6.1 Problem Statement 136
6.2 Test Architecture and Current Solution 137
6.3 Proposed Scheduling Strategies 140
6.3.1 Scheduling Strategy for SoC Dies with Dedicated Wrappers 140
6.3.2 Scheduling Strategy for Extremely Large SoC Dies 142
6.4 Schedule Optimization 146
6.4.1 Sharing of Inputs 146
6.4.2 Output Removal 148
6.5 Subgroup Configuration 149
6.5.1 Independent Subgroup Configuration 150
6.5.2 Dependent Subgroup Configuration 151
6.6 Experimental Results 153
6.6.1 Compression Ratio Analysis 154
6.6.2 Scheduling Results 156
6.6.3 Optimization Results 158
6.6.4 Run-Time Analysis 160
6.7 Conclusion 160
References 161

7 A Programmable Method for Low-Power Scan Shift in SoC Dies 163
7.1 Problem Statement 164
7.2 Related Prior Work and Shift-Clock Staggering 164
7.2.1 Low-Power Testing 165
7.2.2 Principle of Shift-Clock Staggering 165
7.3 Optimization Problem and Exact Solution 167
7.4 Proposed Heuristic Algorithm 169

7.5 Experimental Results 171
7.5.1 Assignment Results 171
7.5.2 Evaluation of Shift-Clock Staggering Using Silicon Data 174
7.6 Conclusion 177
References 178

8 Conclusions 179
8.1 Book Summary 179
8.2 Future Directions 180
References 182