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Architecture of Computing Systems – ARCS 2015

28th International Conference
Porto, Portugal, March 24–27, 2015
Proceedings

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Preface

The 28th International Conference on Architecture of Computing Systems (ARCS 2015) was hosted by the CISTER Research Center at Instituto Superior de Engenharia do Porto, Portugal, from March 24 to 27, 2015 and continues the long-standing ARCS tradition of reporting top-notch results in computer architecture and related areas. It was organized by the special interest group on 'Architecture of Computing Systems' of the GI (Gesellschaft für Informatik e. V.) and ITG (Informationstechnische Gesellschaft im VDE), with GI having the financial responsibility for the 2015 edition. The conference was also supported by IFIP (International Federation of Information Processing).

The special focus of ARCS 2015 was on "Reconciling Parallelism and Predictability in Mixed-Critical Systems." This reflects the ongoing convergence between computational, control, and communication systems in many application areas and markets. The increasingly data-intensive and computational nature of Cyber-Physical Systems is now pushing for embedded control systems to run on complex parallel hardware. System designers are squeezed between the hammer of dependability, performance, power and energy efficiency, and the anvil of cost. The latter is typically associated with programmability issues, validation and verification, deployment, maintenance, complexity, portability, etc. Traditional, low-level approaches to parallel software development are already plagued by data races, non-reproducible bugs, time unpredictability, non-composability, and unscalable verification. Solutions exist to raise the abstraction level, to develop dependable, reusable, and efficient parallel implementations, and to build computer architectures with predictability, fault tolerance, and dependability in mind. The Internet of Things also pushes for reconciling computation and control in computing systems. The convergence of challenges, technology, and markets for high-performance consumer and mobile devices has already taken place. The ubiquity of safety, security, and dependability requirements meets cost efficiency concerns. Long-term research is needed, as well as research evaluating the maturity of existing system design methods, programming languages and tools, software stacks, computer architectures, and validation approaches. This conference put a particular focus on these research issues.

The conference attracted 45 submissions from 22 countries. Each paper was assigned to at least three Program Committee Members for reviewing. The Committee selected 19 submissions for publication with authors from 11 countries. These papers were organized into six sessions covering topics on hardware, design, applicatrions, trust and privacy, and real-time issues. A session was dedicated to the three best paper candidates of the conference. Three invited talks on "The Evolution of Computer Architectures: A View from the European Commission" by Sandro D'Elia, European Commission Unit "Complex Systems & Advanced Computing," Belgium, "Architectures for Mixed-Criticality Systems based on Networked Multi-Core Chips" by Roman Obermaisser, University of Siegen, Germany, and "Time Predictability in High-Performance Mixed-Criticality Multicore Systems" by Francisco Cazorla,

Barcelona Supercomputing Center, Spain, completed the strong technical program. Four workshops focusing on specific sub-topics of ARCS were organized in conjunction with the main conference, one on Dependability and Fault Tolerance, one on Multi-Objective Many-Core Design, one on Self-Optimization in Organic and Autonomic Computing Systems, as well as one on Complex Problems over High Performance Computing Architectures. The conference week also featured two tutorials, on CUDA tuning and new GPU trends, and on the Myriad2 architecture, programming and computer vision applications.

We would like to thank the many individuals who contributed to the success of the conference, in particular the members of the Program Committee as well as the additional external reviewers, for the time and effort they put into reviewing the submissions carefully and selecting a high-quality program. Many thanks also to all authors for submitting their work. The workshops and tutorials were organized and coordinated by João Cardoso, and the poster session was organized by Florian Kluge and Patrick Meumeu Yomsi. The proceedings were compiled by Thilo Pionteck, industry liaison performed by Sascha Uhrig and David Pereira, and conference publicity by Vincent Nélis. The local arrangements were coordinated by Luis Ferreira. Our gratitude goes to all of them as well as to all other people, in particular the team at CISTER, which helped in the organization of ARCS 2015.

January 2015

Luís Miguel Pinho
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Invited Talks

Dr. Sandro D'Elia, European Commission Unit "Complex Systems and Advanced Computing"

The Evolution of Computer Architectures: A view from the European Commission

Abstract of Talk: The changes in technology and market conditions have brought, in recent years, a significant evolution in the computer architectures. Multi-core chips force programmers to think parallel in any application domain, heterogeneous systems integrating different specialised processors are now the rule also in consumer markets, and energy efficiency is an issue across the entire computing spectrum from the wearable device to the high performance cluster. These trends pose significant issues: software development is a bottleneck because efficient programming for parallel and heterogeneous architectures is difficult, and application development remains a labour-intensive and expensive activity; non-deterministic timing in multicore chips poses a huge problem whenever a guaranteed response time is needed; software is typically not aware of the energy it uses, and therefore does not use hardware efficiently. Security is a cross-cutting problem, which in some cases is addressed through hardware-enforced "secure zones". This presentation discusses the recent evolution in computing architectures focusing on examples from European research and innovation projects, with a look forward to some promising innovations in the field like bio-inspired, probabilistic and approximate computing.

Dr. Sandro D'Elia is Project Officer at the European Commission Unit A/3 "Complex Systems & Advanced Computing". He spent a significant part of his career as IT project manager, first in the private sector and then in the IT service of the European Commission. In 2009 he moved to a position of research project officer. His role is evaluating, negotiating, controlling and supporting research and innovation projects financed by the European Commission, contributing to the drafting of the research and innovation work programme, and contributing to European policies on software, cyber-physical systems and advanced computing.

Prof. Dr. Roman Obermaisser, University of Siegen

Architectures for Mixed-Criticality Systems Based on Networked Multi-Core Chips

Abstract of Talk: Mixed-criticality architectures with support for modular certification make the integration of application subsystems with different safety assurance levels both technically and economically feasible. Strict segregation of these subsystems is a key requirement to avoid fault propagation and unintended side-effects due to integration. Also, mixed-criticality architectures must deal with the heterogeneity of subsystems that differ not only in their criticality, but also in the underlying computational models and the timing requirements. Non safety-critical subsystems often demand adaptability and support for dynamic system structures, while certification standards impose static configurations for safety-critical subsystems. Several aspects such as time and space partitioning, heterogeneous computational models and adaptability were individually addressed at different integration levels including distributed systems, the chip-level and software execution environments. However, a holistic architecture for the seamless mixed-criticality integration encompassing distributed systems, multi-core chips, operating systems and hypervisors is an open research problem. This presentation discusses the state-of-the-art of mixed-criticality systems and presents research challenges towards a hierarchical mixed-criticality platform with support for strict segregation of subsystems, heterogeneity and adaptability.

Prof. Dr. Roman Obermaisser is full professor at the Division for Embedded Systems at University of Siegen in Germany. He has studied computer sciences at Vienna University of Technology and received the Master's degree in 2001. In February 2004, Roman Obermaisser has finished his doctoral studies in Computer Science with Prof. Hermann Kopetz at Vienna University of Technology as research advisor. In July 2009, Roman Obermaisser has received the habilitation ("Venia docendi") certificate for Technical Computer Science. His research work focuses on system architectures for distributed embedded real-time systems. He is the author of numerous conference and journal publications. He also wrote books on cross-domain system architectures for embedded systems, event-triggered and time-triggered control paradigms and time-triggered communication protocols. He has also participated in several EU research projects (e.g. DECOS, NextTTA, universAAL) and was the coordinator of the European research projects GENESYS and ACROSS. At present Roman Obermaisser coordinates the European research project DREAMS that will establish a mixed-criticality architecture for networked multi-core chips.

Dr. Francisco Cazorla, Barcelona Supercomputing Center

Time Predictability in High-Performance Mixed-Criticality Multicore Systems

Abstract of Talk: While the search for high-performance will continue to be one of the main driving factors in computer design and development, there is an increasing need for time predictability across computing domains including high-performance (datacentre and supercomputers), handheld and embedded devices. The trend towards using computer systems to increasingly control essential aspects of human beings and the increasing connectivity across devices will naturally lead to situations in which applications - partially executed in handheld and datacentre computers, directly connect with more embedded critical systems such as cars or medical devices. The problem lies in the fact that high-performance is usually achieved by deploying aggressive hardware features (speculation, caches, heterogeneous designs) that negatively impact time predictability. The challenge lies on finding hardware/software designs that balance high-performance and time-predictability as needed by the application environment. In this talk I will focus on the increasing needs of time predictability in computing systems. I will present some of the main challenges in the design of multicores and manycores, widely deployed in the different computer domains, to provide increasing degrees of time predictability without significantly degrading average performance. I will present the work done in my research group in two different directions to reach this goal, namely, probabilistic multicore systems and the analysis of COTS multicore processors.

Dr. Francisco J. Cazorla is a researcher at the National Spanish Research Council (CSIC) and the leader of the CAOS research group (Computer Architecture - Operating System) at the Barcelona Supercomputing Centre (www.bsc.es/ caos). His research area covers the design for both high-performance and real-time systems. He has led several research projects funded by industry including several processor vendor companies (IBM, Sun microsystems) and the European Space Agency. He has also participated in European FP6 (SARC) and FP7 Projects (MERASA, parMERASA). He led the FP7 PROARTIS project and currently leads the FP7 PROXIMA project. He has co-authored over 70 papers in international refereed conferences and has several patents on the area.

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