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A Pipelined Multi-core MIPS Machine

Hardware Implementation and Correctness Proof

Springer

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Preface

This book is based on the third author's lectures on computer architecture, as given in the summer semester of 2013 at Saarland University. It contains a gate level construction of a multi-core machine with pipelined MIPS processor cores and a sequentially consistent shared memory. This opens the way to the formal verification of synthesizable hardware for multi-core processors in the future.

We proceed in three steps: i) we review pipelined single core processor constructions and their correctness proofs, ii) we present a construction of a cache-based shared memory which is kept consistent by the MOESI protocol and show that it is sequentially consistent, and iii) we integrate the pipelined processor cores into the shared memory and show that the resulting hardware simulates the steps of an abstract multi-core MIPS machine in some order. In the last step the reference machine consists of MIPS cores and a single memory, where the cores, together with the shared memory, execute instructions in a nondeterministic order.

In the correctness proofs of the last two steps a new issue arises. Constructions are in a gate level hardware model and thus deterministic. In contrast the reference models against which correctness is shown are nondeterministic. The development of the additional machinery for these proofs and the correctness proof of the shared memory at the gate level are the main technical contributions of this work.

October 2014

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