

Analog Circuits and Signal Processing

Volume 128

Series editors

Mohammed Ismail, The Ohio State University, USA

Mohamad Sawan, École Polytechnique de Montréal, Canada

More information about this series at <http://www.springer.com/series/7381>

Valentijn De Smedt · Georges Gielen
Wim Dehaene

Temperature- and Supply Voltage-Independent Time References for Wireless Sensor Networks

 Springer

Valentijn De Smedt
Georges Gielen
Wim Dehaene
ESAT-MICAS
University of Leuven
Heverlee
Belgium

ISSN 1872-082X
ISBN 978-3-319-09002-3
DOI 10.1007/978-3-319-09003-0

ISSN 2197-1854 (electronic)
ISBN 978-3-319-09003-0 (eBook)

Library of Congress Control Number: 2014945254

Springer Cham Heidelberg New York Dordrecht London

© Springer International Publishing Switzerland 2015

This work is subject to copyright. All rights are reserved by the Publisher, whether the whole or part of the material is concerned, specifically the rights of translation, reprinting, reuse of illustrations, recitation, broadcasting, reproduction on microfilms or in any other physical way, and transmission or information storage and retrieval, electronic adaptation, computer software, or by similar or dissimilar methodology now known or hereafter developed. Exempted from this legal reservation are brief excerpts in connection with reviews or scholarly analysis or material supplied specifically for the purpose of being entered and executed on a computer system, for exclusive use by the purchaser of the work. Duplication of this publication or parts thereof is permitted only under the provisions of the Copyright Law of the Publisher's location, in its current version, and permission for use must always be obtained from Springer. Permissions for use may be obtained through RightsLink at the Copyright Clearance Center. Violations are liable to prosecution under the respective Copyright Law. The use of general descriptive names, registered names, trademarks, service marks, etc. in this publication does not imply, even in the absence of a specific statement, that such names are exempt from the relevant protective laws and regulations and therefore free for general use.

While the advice and information in this book are believed to be true and accurate at the date of publication, neither the authors nor the editors nor the publisher can accept any legal responsibility for any errors or omissions that may be made. The publisher makes no warranty, express or implied, with respect to the material contained herein.

Printed on acid-free paper

Springer is part of Springer Science+Business Media (www.springer.com)

*The only reason for time is so that
everything doesn't happen at once.*

–A. Einstein

Preface

“Most of what makes a book ‘good’ is that we are reading it at the right moment for us” is a quote from the Swiss-British philosopher Alain De Botton. The quote is right on top for a book where timing is the central given. Read this book about timing if at this moment your design is in need of an accurate yet efficient timing reference!

The book you are holding is the result of several years of Ph.D. research that started with the ambition to set important steps toward the implementation of batteryless wireless sensor nodes. Relatively soon it became clear that accurate timing is one of the key points in realizing this. Therefore the focus shifted to the construction of a low power, supply, and/or temperature independent timing reference. This topic in its turn surpasses the world of wireless sensor networks as it is much wider applicable.

We are convinced that the results we present here can help you in several ways. You can have a look at the circuits and concepts and adapt them for your system. More importantly the book can act as a source of inspiration for all those that are involved in sensor network design and the hardware for the Internet of Things. We dare to hope that the book brings you as much research inspiration as it brought us research joy while creating it.

Leuven, September 2014

Valentijn De Smedt
Georges Gielen
Wim Dehaene

Contents

1	Introduction	1
1.1	Historical Introduction	1
1.1.1	Electromagnetic Transmission	3
1.1.2	The Vacuum Tube	8
1.1.3	The Invention of the Transistor	11
1.2	Wireless Sensor Networks	17
1.2.1	RFID Adoption	17
1.2.2	Challenges in RFID Design	18
1.2.3	The Pinballs Framework	18
1.2.4	Architecture of an RFID Tag	23
1.3	Focus and Outline of this Work	26
Part I Theoretical Background on Oscillators and Time References		
2	Oscillators and Time References	31
2.1	Introduction	31
2.2	The Phase Space Description of an Oscillator	32
2.2.1	The Phase Space Description	32
2.2.2	One-Dimensional Systems	32
2.2.3	Two-Dimensional Systems	34
2.2.4	The van der Pol Oscillator	36
2.2.5	n-Dimensional Systems	39
2.3	Minimum Requirements for a Time Reference	42
2.3.1	An Energy Reservoir and a Resistor	43
2.3.2	Two Different Energy Reservoirs	44
2.3.3	Harmonic Versus Relaxation Oscillators	46

2.4	Representation of an Oscillator Signal	47
2.4.1	Oscillator Signals in the Time Domain	47
2.4.2	Oscillator Signals in the Frequency Domain	49
2.5	Properties of an Oscillator	52
2.5.1	The Quality Factor	53
2.5.2	Stability of an Oscillator Signal	59
2.6	Conclusion.	59
3	Jitter and Phase Noise in Oscillators	61
3.1	Introduction	61
3.2	Noise Sources	62
3.2.1	Noise in a Resistor	63
3.2.2	Noise in a P-N Junction.	63
3.2.3	MOS Transistor Noise.	64
3.3	The Phase Noise Spectrum.	64
3.3.1	The Noise Model of Leeson.	65
3.4	The Phase Noise Theory of Hajimiri	68
3.4.1	Generation of the Phase Noise Spectrum	68
3.4.2	Extensions to the Theory of Hajimiri.	74
3.4.3	Calculation of the ISF	76
3.4.4	Evaluation of Hajimiri's Theory	78
3.5	Nonlinear Noise Theories.	79
3.5.1	The Lorentzian Spectrum.	79
3.5.2	The Gaussian Spectrum	80
3.5.3	Evaluation	81
3.6	Phase Noise Versus Jitter.	82
3.6.1	Definition of Jitter	82
3.6.2	Only White Noise Sources.	85
3.6.3	Colored Noise Sources	85
3.6.4	General Calculation Method.	86
3.7	The Q Factor and the Noise	87
3.7.1	The Theory of Leeson.	87
3.7.2	The Theory of Hajimiri	87
3.8	Figures of Merit	88
3.8.1	The Phase Noise FoM.	88
3.9	Conclusion.	90
4	Long-term Oscillator Stability	91
4.1	Introduction	91
4.1.1	Causes of Frequency Drift	91
4.1.2	Organization of this Chapter.	92
4.2	Building Blocks of an Oscillator.	92
4.2.1	Linear Oscillator Systems	93

- 4.2.2 Nonlinear Oscillator Systems 94
- 4.2.3 Transistor Behavior 100
- 4.2.4 Properties of the Feedback Network 102
- 4.2.5 How to Obtain a Stable Oscillator? 106
- 4.3 Figures of Merit for Long-term Stability 108
 - 4.3.1 Temperature FoM 108
 - 4.3.2 Supply Voltage FoM 109
- 4.4 Oscillators for Low-Power Applications 110
 - 4.4.1 Harmonic Integrated Oscillators 113
 - 4.4.2 Relaxation Integrated Oscillators 121
 - 4.4.3 Ring Oscillators 127
 - 4.4.4 Other Implementations 129
 - 4.4.5 Comparison of the Different Topologies 133
- 4.5 Conclusion 135

Part II Oscillator Designs for Temperature and Voltage Independence

- 5 Design of Two Wien Bridge Oscillators 139**
 - 5.1 Introduction 139
 - 5.1.1 The Wien Bridge Oscillator 140
 - 5.2 The Temperature-Independent Wien Bridge 141
 - 5.2.1 Basic Amplifier Structure 142
 - 5.2.2 The Amplitude Regulator 146
 - 5.2.3 Complete Circuit 148
 - 5.2.4 Phase Noise Performance 148
 - 5.2.5 Measurement Results 155
 - 5.2.6 Conclusion on the Temperature-Independent Wien Bridge Oscillator 158
 - 5.3 The Supply Voltage-Independent Wien Bridge Oscillator 159
 - 5.3.1 The Oscillator Topology 160
 - 5.3.2 The Proposed Oscillator 161
 - 5.3.3 The LDO Regulator 164
 - 5.3.4 Temperature Dependency of the Voltage-Independent Oscillator 167
 - 5.3.5 Measurement Results 169
 - 5.3.6 Conclusion on the Voltage-Independent Oscillator 172
 - 5.4 General Conclusion 172
- 6 The Pulsed Oscillator Topology 173**
 - 6.1 Introduction 173
 - 6.2 The Pulsed-Harmonic Oscillator Topology 174
 - 6.2.1 The Energy Tank 175

6.3	Transient Behavior of the Energy Tank	176
6.3.1	The n -th Order Transfer Function	177
6.3.2	Realistic Second-Order Tanks	179
6.4	Behavior of the Pulsed LC Oscillator	183
6.4.1	Sensitivity to PW and MoI	186
6.4.2	Energy Losses During Oscillation	188
6.5	Phase Noise in the Pulsed LC Oscillator	189
6.5.1	Noise Injection During the Free-Running Period	189
6.5.2	Noise Injection During the Applied Pulse	193
6.5.3	Impact of the Different Noise Sources	194
6.6	Implementation of the Pulsed LC Oscillator	196
6.6.1	Design of the LC Tank	196
6.6.2	Design of the Differential Amplifier	198
6.6.3	The Counter	200
6.6.4	The Pulse Generator	200
6.7	Measurement Results	202
6.8	Conclusion	207
7	Injection-Locked Oscillators	209
7.1	Introduction	209
7.2	Injection Locking of an Oscillator	211
7.2.1	Lock Range of the Oscillator	211
7.2.2	Dynamic Behavior of the Locking Process	216
7.2.3	Frequency Beating	220
7.3	Phase Noise in the Injection-Locked Oscillator	222
7.3.1	Noise Model Using a Decreased Tank Impedance	223
7.3.2	A PLL-Based Noise Model	225
7.4	The Wirelessly-Locked Oscillator in 130 nm	229
7.4.1	The Oscillator Topology	229
7.4.2	Techniques to Increase the Lock Range	233
7.4.3	Measurement Results	236
7.4.4	Conclusion on the 130-nm Injection-Locked Oscillator	237
7.5	The 40-nm Injection-Locked Receiver	238
7.5.1	The Clock Circuit	240
7.5.2	The Receiver Circuit	247
7.5.3	Measurement and Simulation Results	250
7.6	Conclusion	256
8	Oscillator-Based Sensor Interfaces	257
8.1	Introduction	257
8.2	PLL-Based Sensor Interfaces	258
8.2.1	Implementation of the PLL	258

- 8.3 The PWM-Based Sensor Interface 260
 - 8.3.1 The Coupled Sawtooth Oscillator 261
 - 8.3.2 Use in Combination with a Sensor 263
 - 8.3.3 Transmission of the Output Signal 265
- 8.4 Jitter in the Coupled Sawtooth Oscillator 266
 - 8.4.1 Jitter due to Sensor Noise 267
 - 8.4.2 Jitter from the Differential Pair 270
 - 8.4.3 Jitter due to the Current Source 272
 - 8.4.4 Noise Propagation to the Sensor Interface Output 273
 - 8.4.5 A/D-Converter FoM 277
- 8.5 Implementation of the Sensor Interface 278
 - 8.5.1 Implementation in 130 nm CMOS 278
 - 8.5.2 Implementation in 40 nm CMOS 282
 - 8.5.3 Measurement Results. 288
- 8.6 Conclusion. 292

Part III Wireless Sensor Nodes

- 9 Design of a Low-Power Wireless RFID Tag 295**
 - 9.1 Introduction 295
 - 9.2 Architecture of the Wireless Tag. 296
 - 9.2.1 The Clock and Receiver Circuit 297
 - 9.2.2 The UWB Transmitter. 298
 - 9.2.3 The Sensor Interface 299
 - 9.2.4 The Digital Logic 300
 - 9.3 Measurement Results. 302
 - 9.4 Conclusion. 305
- 10 Conclusion 307**
 - 10.1 Comparison to the State of the Art 308
 - 10.1.1 The Wien Bridge Implementations 308
 - 10.1.2 The Pulsed-Harmonic Oscillator 309
 - 10.1.3 The Injection-Locked Oscillators. 311
 - 10.1.4 The Sensor Interface 311
 - 10.1.5 The Wireless Tag 312
 - 10.1.6 General Conclusions 312
 - 10.2 Main Contributions 313
 - 10.3 Suggestions for Future Work 314

**Appendix A: Definitions and Conventions Used
Throughout the Work 317**

Appendix B: Influence of a Nonlinear Amplifier 331

Appendix C: Measurement Issues for Jitter and Phase Noise. 341

Appendix D: Comparison to the State of the Art. 353

References. 361

Index 377

Abstract

Back in 2000, the Nobel prize committee recognized the invention of the integrated circuit in 1958 by Jack Kilby as one of the most far-reaching steps forward in modern technology. Today, almost 60 years after this invention, electronics are found everywhere in our society. This is mainly caused by the characteristic exponential growth factors in the electronics industry (Moore's law), which result in an exponential miniaturization and cost decrease. This evolution goes hand in hand with a similar growth of wireless communication technology: devices become smaller, frequencies and data rates higher. As a result, the wearability and functionality of wireless electronic devices drastically increase.

This ongoing technological progress is a direct cause of the appearance of Wireless Sensor Networks (WSN). An increasing number of autonomously operating devices is wirelessly connected to a network and/or to the Internet, an evolution which will eventually result in the so-called Internet of Things. Since both the miniaturization as well as the cost decrease of these wireless sensor nodes is necessary to become economically feasible, a growing need for fully-integrated, single-chip wireless devices is observed. The use of modern deep-submicron CMOS technologies in analog electronics, however, has several drawbacks in terms of temperature sensitivity and linearity.

This work elaborately investigates the possible circuit techniques to overcome the temperature and supply voltage sensitivity of fully integrated time references for ultra-low-power wireless communication in WSN. In a first step, the basic needs to build a frequency reference are studied. Furthermore, a closer look at the short-term as well as the long-term frequency stability of integrated oscillators is taken. This results in a design strategy, which is applied to six different oscillator design cases. All six implementations are subject to a study of phase noise and long-term frequency stability.

The first two implementations are respectively a temperature- and a supply voltage-independent Wien bridge oscillator. The temperature independence is obtained by using a novel feedback amplifier topology of which the output resistance only depends on a temperature stable resistor. This requires advanced circuit techniques and a highly-stable amplitude regulation circuit. The second Wien

bridge implementation makes use of two nested regulators, resulting in an ultra-high supply voltage stability over a wide voltage range.

The third design case makes use of a high-quality bondwire LC tank. A novel pulsed driving technique is developed to decrease the power consumption of the high-frequency oscillator circuit. This driving technique reduces the impact of the oscillator circuitry on the output frequency and therefore also on the temperature- and supply voltage stability of the oscillator. To better understand the application field of the pulsed oscillator topology, the noise performance is analyzed as well. The processed implementation is a unique combination of power consumption and long-term frequency stability.

Next, two injection-locked oscillator implementations are discussed. Apart from a stable output frequency, a high absolute accuracy is also obtained due to the locking to a wirelessly received RF signal. The first design uses the received 2.4 GHz carrier frequency as a time reference. Despite its simple system topology, this approach has several drawbacks in terms of selectivity and power consumption. The second implementation locks to the envelope of the received RF signal. Therefore, the oscillator can run at a low frequency, drastically diminishing the power consumption. A second improvement is the addition of a network coordination receiver. For this purpose, a novel ultra-low-power receiver topology and demodulation technique are developed. As a result of the addressability, the overall power consumption in the network is reduced.

The last design case is a temperature- and supply voltage-independent oscillator-based sensor interface. Since the challenge in this design is rather the stability of the output value than the frequency stability, a different design strategy is used. It is shown that the matching of different oscillator delay stages can be applied to obtain a stable and highly-linear digitalization of a sensor input.

The wirelessly injection-locked oscillator, the coordination receiver, the sensor interface, and a transmitter are combined into one highly-flexible wireless tag. The content, the scrambling code, and the length of the transmitted data burst can be adapted freely, depending on the application. The developed tag can therefore be used in a wide range of applications, with different accuracy requirements and energy constraints.

Finally, an elaborate comparison between the developed oscillator designs and the state of the art is performed. It is shown that the free-running implementations as well as the injection-locked designs improve the state of the art. This discussion results in several suggestions for possible future work.

About the Authors



Valentijn De Smedt (S'08) was born in Lubbeek, Belgium, in 1984. He received the M.Sc. degree in electrical engineering from the Katholieke Universiteit Leuven in 2007. The subject of his Master thesis was the design of an accurate integrated frequency reference. From 2007 to 2014 he was working as a research assistant at the MICAS laboratories of the Katholieke Universiteit Leuven towards a Ph.D. degree on the design of ultra-low-power time-based building blocks for wireless sensor networks, which he received in April 2014. At KU Leuven, he was involved in and has set up several extra-curricular

educational projects, some of them in co-operation with the IEEE Student Branch of Leuven.

He has been vice-chair technical activities of the IEEE student branch of Leuven between 2009 and 2013 and chaired the IEEE Student Branch and GOLD congress 2010 (SBC 2010). Since 2011, he is IEEE Benelux GOLD (Young Professionals) chair and co-chair of the IEEE SSCS Benelux chapter. Since 2009 he is a guest lecturer at ACE Group-T on UWB standards and Zigbee.



Georges G.E. Gielen received the M.Sc. and Ph.D. degrees in Electrical Engineering from the Katholieke Universiteit Leuven (KU Leuven), Belgium, in 1986 and 1990, respectively. He is a full professor at the Department of Electrical Engineering (ESAT). From August 2013, Georges Gielen is also appointed as vice-rector for the Group Science, Engineering and Technology and Academic Personnel of the KU Leuven.

His research interests are in the design of analog and mixed-signal integrated circuits, and especially in analog and mixed-signal CAD tools and design automation. He is a coordinator or partner of several (industrial) research projects in this area, including several European projects. He has authored or coauthored seven books and more than 450 papers in edited books, international journals, and conference proceedings. He is a Fellow of the IEEE since 2002.



Wim Dehaene was born in Nijmegen, The Netherlands, in 1967. He received the M.Sc. degree in electrical and mechanical engineering in 1991 from the Katholieke Universiteit Leuven. In November 1996, he received the Ph.D. degree at the Katholieke Universiteit Leuven. His thesis is entitled “CMOS integrated circuits for analog signal processing in hard disk systems.”

After receiving the M.Sc. Degree, Wim Dehaene was a research assistant at the ESAT-MICAS Laboratory of the Katholieke Universiteit Leuven. His research involved the design of novel CMOS building blocks for hard disk systems. The research was first sponsored by the IWONL (Belgian Institute for Science and Research in Industry and Agriculture) and later by the IWT (the Flemish institute for Scientific Research in the Industry). In November 1996, Wim Dehaene joined Alcatel Microelectronics, Belgium. There he was a senior project leader for the feasibility, design and development of mixed mode systems on chip. The application domains were telephony, xDSL, and high-speed wireless LAN. In July 2002, Wim Dehaene joined the staff of the ESAT-MICAS Laboratory of the Katholieke Universiteit Leuven where he is now a full professor. His research domain is circuit level design of digital circuits. The current focus is on ultra low power signal processing and memories in advanced CMOS technologies. Part of this research is performed in cooperation with IMEC, Belgium where he is also a part-time principal scientist.

Wim Dehaene is teaching several classes on electrical engineering and digital circuit and system design. He is also very interested in the didactics of engineering. As such, he is guiding several projects aiming to bring engineering to youngsters and he is a teacher in the teacher education program of the KU Leuven.

Wim Dehaene is a senior member of the IEEE. Wim Dehaene is a member of the technical program committee of ESSCIRC and ISSCC.

Abbreviations

A-ISF	Amplitude Impulse Sensitivity Function
AC	Alternating Current
AM	Amplitude Modulation
BBPLL	Bang–Bang Phase-Locked Loop
BER	Bit Error Rate
BJT	Bipolar Junction Transistor
CMB	Cosmic Microwave Background
DAC	Digital-to-Analog Converter
EEF	Energy Enhancement Factor
ELP	Extremely-Low Power
ENOB	Effective Number of Bits
ETF	Electro-Thermal Filter
FET	Field-Effect Transistor
FLL	Frequency-Locked Loop
FoM	Figure of Merit
FRS	Fellow of the Royal Society
FSM	Finite State Machine
IFF	Identification Friend or Foe
IoT	Internet of Things
IR-UWB	Impulse Radio Ultra-Wideband
ISF	Impulse Sensitivity Function
JFET	Junction Field-Effect Transistor
LDO	Low-DropOut
LFSR	Linear Feedback Shift Register
LTI	Linear Time-Invariant
LTV	Linear Time-Variant
MEMS	Microelectromechanical systems
MiM	Metal-insulator-Metal

MoI	Moment of Impact
MoM	Metal-oxide-Metal
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
OCXO	Oven-Compensated Crystal Oscillator
P-UWB	Pulsed Ultra-Wideband
PC	Personal Computer
pcb	Printed Circuit Board
PDF	Probability Density Function
ppb	Parts per billion
ppm	Parts per million
PSD	Power Spectral Density
PVT	Process, Temperature and (Supply) Voltage
PW	Pulse Width
RF	Radio Frequency
RFID	Radio Frequency Identification
rms	Root mean square
SNDR	Signal to Noise and Distortion Ratio
SNR	Signal to Noise Ratio
TANSTAAFL	There Ain't No Such Thing As A Free Lunch
TCXO	Temperature-Compensated Crystal Oscillator
ULP	Ultra-Low Power
VCO	Voltage-Controlled Oscillator
VCXO	Voltage-Controlled Crystal Oscillator
WSN	Wireless Sensor Network
XO	Crystal Oscillator

Symbols

$\alpha(\omega \cdot t)$	Deterministic, periodic function with period 2π
α_k	Phase shift of the k -th harmonic of a voltage oscillator signal
α_{μ_n}	Temperature coefficient of the electron mobility
$\alpha_{V_{th}}$	Temperature coefficient of the transistor threshold voltage
β	Phase modulation index
β_k	Phase shift of the k -th harmonic of a voltage oscillator signal
$\Delta\omega_{3dB}$	–3 dB width of a resonant peak in a transfer function
Δf_{-3dB}	Half-power width of an oscillator output spectrum
ΔT_n	Delay error induced by noise
ΔV_n	Output voltage error induced by noise
ΔV_{rel}	Relative supply voltage span, as defined in Sect. 4.3.2
$\mathcal{A}(\Delta\omega)$	Amplitude noise density at frequency offset $\Delta\omega$, relative to the carrier
$\Delta\omega_0$	Difference between the fundamental frequency ω_0 and the natural frequency ω_n of the tuned network
$\Delta\omega_n$	Angular frequency difference between the natural oscillator frequency ω_n and the frequency of an injected signal ω_i
$\Delta\omega_{inj}$	Frequency perturbation on the injected signal i_{inj} , equal to $d\phi_{inj}(t)/dt$
$\Delta\omega_{nn}$	Frequency perturbation on the free-running oscillator signal (not the injection-locked oscillator signal), equal to $d\phi_{nn}(t)/dt$
$\Delta\phi_i(t)$	Perturbation of the phase shift between an oscillator current and an injected current (due to noise), equal to $\Delta\phi_{inj}(t) - \Delta\phi_{osc}$
$\Delta\phi_{inj}(t)$	Perturbation on the phase of the injected signal i_{inj}
$\Delta\phi_{osc}$	Perturbation on the phase of the (locked) oscillator signal

δ_k	Relative amplitude of the k -th harmonic of the voltage waveform, compared to the amplitude of the fundamental frequency
δ_{Xx}	Skin-depth of a conducting material Xx (for instance Silver, Ag)
ε	Parameter equal to A_{inj}/A_{osc}
$\varepsilon(t)$	Random amplitude variation of an oscillator signal
γ	Constant parameter used to determine the bandwidth of a Lorentzian spectrum, equal to $\pi \cdot f_0^2 \cdot c$
$\Gamma(x)$	The Impulse Sensitivity Function (ISF) with period $2 \cdot \pi$
$\Gamma_i(x)$	Impulse Sensitivity Function (ISF) on node i with period $2 \cdot \pi$
γ_k	Relative amplitude of the k -th harmonic of the voltage waveform, compared to the amplitude of the fundamental frequency
$\Gamma_{eff}(x)$	Effective Impulse Sensitivity Function (ISF), taking cyclostationary noise sources into account
Γ_{rms}	Root mean square (rms) value of the Impulse Sensitivity Function (ISF)
$A(x)$	Amplitude Impulse Sensitivity function (A-ISF), with period $2 \cdot \pi$
λ_i	Eigenvalue with corresponding eigenvector \mathbf{u}_i
$A_i(x)$	Amplitude Impulse Sensitivity function (A-ISF) on node i , with period $2 \cdot \pi$
ρ	Generalized eigenvector with corresponding eigenvalue λ
μ	Scalar nonlinearity parameter in the <i>van der Pol</i> equation
μ_{Xx}	Magnetic permeability of a conducting material Xx (for instance Silver, Ag)
Ω	Unit of electrical resistance
ω	Instantaneous angular frequency, pulsation, $2\pi f$
$\omega(t)$	Instantaneous angular frequency over time
ω_0	Constant mean angular frequency of an oscillator, often used as the angular frequency in standard conditions
ω_B	Beating frequency of an injected oscillator
ω_i	Angular frequency of an injected signal
ω_L	One-sided lock range of an injection-locked oscillator
ω_m	Angular frequency of a motor
ω_n	Natural angular frequency of an electrical (tuned) network, natural angular frequency of an oscillator, $2\pi f_n$
Φ	magnetic flux due to the magnetic poles in a motor
$\Phi(t)$	Instantaneous phase of an oscillator signal
$\phi(t)$	Random variations of noise in the phase function, also called excess phase function
ϕ_∞	Steady-state phase shift between the oscillator current and the injected current

$\phi_i(t)$	Phase shift between the oscillator current and the injected current
ϕ_{ETF}	Phase shift of an Electro-Thermal Filter
$\phi_{i,0}$	Initial phase shift between the oscillator current and the injected current
$\phi_{inj}(s)$	Phase shift of the injected signal in the frequency domain
$\phi_{nm}(s)$	Phase shift of the free-running oscillator signal in the frequency domain
$\phi_{nm}(t)$	Phase shift of the free-running oscillator signal (not the injection-locked oscillator signal)
$\phi_{osc}(s)$	Phase shift of the locked oscillator signal in the frequency domain
ψ	Phase shift between the injected signal and the relaxation oscillator current
$\Psi(t)$	Systematic or deterministic variations in the phase function
ρ_{Xx}	Conductivity of a conducting material Xx (for instance Silver, Ag)
$\sigma(A, f, \tau)$	Allan variance of the output of a function f with dead time τ between the subsequent samples
$\sigma(T_h, T_l)$	Covariance between two stochastic periods
σ_c	Cycle-to-cycle jitter of an oscillator output signal
$\sigma_{A,h,l}$	Allan covariance between two variables T_h and T_l (with dead time τ)
$\sigma_{abs}(t = N \cdot \tau_{avg})$	Standard deviation of the absolute jitter after N oscillation cycles, sometimes also called the absolute jitter
σ_{cc}	Alternative definition of the cycle-to-cycle jitter, calculated using the difference between subsequent periods
$\sigma_{LC,Cte}$	Average cycle-to-cycle jitter of the output waveform of a resonant tank with constant output amplitude
$\sigma_{LC,Pulsed,N}$	Standard deviation of the length of the pulsed period of an LC tank, normalized to $T_{LC}/2$
σ_{LC}	Average cycle-to-cycle jitter of the output waveform of a resonant tank with decaying output amplitude
σ_{T_n}	Standard deviation (rms) of the time noise on a stage delay
σ_{V_n}	Standard deviation (rms) of the voltage noise
τ	An arbitrary moment in time
τ_i	Period of the i -th oscillation cycle
τ_{avg}	Average period of an oscillator output signal
$\theta(t)$	Phase shift of an oscillation over time (compared to $\omega_n \cdot t$)
θ_0	Initial phase shift of an oscillation
θ_i	Phase shift induced by a small injected signal in the oscillator, angle between the oscillator signal and the resulting signal
θ_n	Phase shift of a tuned network at $\omega \neq \omega_n$

$\Upsilon(t)$	Deterministic and systematic amplitude variations of an oscillator signal
A	Voltage gain of a generic amplifier
A_0	Ideal constant amplitude of an oscillator signal
A_1	Linear gain of a voltage dependent transconductance amplifier
A	Ampère, unit of electrical current
A_D	Area or size of a diode junction
A_{ds}	Amplitude of the drain-source current in an oscillator
$A_{env,DC}$	DC approximation of the complex envelope of an oscillator output signal
$A_{env}(t)$	Complex envelope of an oscillator output signal
A_i	i -th-order gain of a voltage dependent transconductance amplifier
A_{inj}	Amplitude of a signal injected in an oscillator
A_{osc}	Amplitude of an oscillator signal current
A_R	Area or size of a resistor
A_r	Amplitude of the resulting oscillator signal, sum of the injected current and the oscillator current
$A(t)$	Instantaneous amplitude of an oscillator signal
A_t	Minimum attenuation of a feedback network
A_v	Voltage gain of an amplifier
B	Bandwidth of a modulating signal
C	Capacitance, a capacitor
c	Motor constant, speed of light
c	Constant parameter used to determine the bandwidth of a Lorentzian spectrum
C_{ds}	Drain-source capacitor of a MOS transistor
C_{gd}	Gate-drain capacitor of a MOS transistor
C_{gs}	Gate-source capacitor of a MOS transistor
c_i	Complex i -th pole frequency
C_{ox}	Gate-oxide capacitance per unit area of a MOS transistor
C_p	Parallel capacitor in the equivalent quartz crystal model
C_s	Series capacitor in the equivalent quartz crystal model
DC	Duty cycle of a digital signal
e	Euler's constant
$E_{Decay}(N)$	Energy loss over N oscillation cycles in a resonant tank with exponentially decaying output amplitude
E_M	Back electromotive force
$E_{Osc}(N)$	Energy loss over N oscillation cycles in a resonant tank with constant output amplitude
$f(\Phi(t))$	Periodic function of $\Phi(t)$ with period $2 \cdot \pi$
F	Device excess noise factor
F_{amp}	Noise factor of an amplifier

F	Farad, unit of electrical capacitance
f_i	State variable of an oscillation on node i , normalized to amplitude and frequency
$f_i(x_1, \dots, x_n)$	A smooth real-valued function of x_1, \dots, x_n
FoM_{AD}	Figure of Merit for Analog to Digital converters
FoM_{JT}	Jitter and Temperature-dependency Figure of Merit (FoM) of an oscillator
FoM_{PN}	Phase noise Figure of Merit (FoM) of an oscillator
$FoM_{PN,tuned}$	Phase noise Figure of Merit (FoM) of an oscillator, taking the tuning sensitivity into account
FoM_{PNT}	Phase noise and Temperature-dependency Figure of Merit (FoM) of an oscillator
FoM_{PNTV}	Phase noise, Temperature-dependency and Voltage-dependency Figure of Merit (FoM) of an oscillator
FoM_{TV}	Temperature- and Voltage-dependency Figure of Merit (FoM) of an oscillator
FoM_V	Voltage-dependency Figure of Merit (FoM) of an oscillator
G	Transconductance of a generic amplifier
g_m	Transconductance of a transistor
g_{mb}	Transconductance of the bulk of a transistor
$G_m(v)$	Gain of a nonlinear negative resistance or amplifier
$g_{m,wi}$	Transconductance of a MOS transistor in weak-inversion
$G(s)$	Transconductance of a generic amplifier, dependent on the Laplace variable (representing the frequency)
$G(v)$	Input-amplitude-dependent transconductance of a generic amplifier
$h_\phi(t, \tau)$	Unit impulse response for the excess phase for a charge injected at time τ
$h_A(t, \tau)$	Unit amplitude impulse response for a charge injected at time τ
H	Henry, unit of electrical inductance
$H_{inj}(j \cdot \Delta\omega)$	Transfer function of the phase perturbations on the injected signal i_{inj} to the injection-locked oscillator output
$H_n(j \cdot \Delta\omega)$	Transfer function of the phase perturbations on the free-running oscillator signal i_{osc} to the injection-locked oscillator output
$h_n(t)$	Normalized impulse response of a resonant network
$H(s)$	Transfer function of a linear system or network
$h(t)$	Impulse response of a linear system or network
I	Unity matrix, symbol of electrical current, mechanical moment of inertia
I_A	Current amplitude through an inductor
I_b	Biasing current of an oscillator or an oscillator stage

I_{D0}	Technology dependent parameter determining the weak-inversion current of a MOS transistor
$i_{d,n}(t)$	Small-signal differential noise current
I_{ds}	Large-signal drain-source current of a MOS transistor
i_{ds}	Small-signal drain-source current of a MOS transistor
$I_{ds,f}$	Zero-temperature-coefficient DC biasing current of a transistor
$I_{ds,wi}$	Large-signal drain-source current of a MOS transistor in weak-inversion
$i_{inj}(t)$	Injected current in an oscillator
$I_{i,reg}$	Regulated output current of a current regulation circuit
$I_{i,reg,rep}$	Regulated output current through the oscillator replica when the regulator is loaded with a resistor
I_k	Fourier coefficient of a current oscillator signal
$\Im(x)$	The imaginary part of x
I_n	Amplitude of a noise current
$i_{n0}(t)$	Stationary current noise source
$i_n(t)$	Injected small-signal noise current
i_{osc}	Oscillator signal current
$i_r(t)$	Resulting current in an oscillator, sum of the injected current and the oscillator current
$I(s)$	Laplace transform of a current waveform
$i(t)$	Small-signal current
j	Imaginary unit, $\sqrt{-1}$
$j_{abs}(t = N \cdot \tau_{avg})$	Absolute jitter after N oscillation cycles
$J(d)$	Current density in a conductor, depending on the distance d from the surface
J	Joule, unit of energy
J_s	Current density in a conductor at the surface
k	The Boltzmann constant, approximately equal to $1.38 \text{ m}^2 \cdot \text{kg} \cdot \text{s}^{-1} \cdot \text{K}^{-1}$
k_{100}	Conversion gain of an envelope detector for an input signal with 100 % modulation depth
k_{30}	Conversion gain of an envelope detector for an input signal with 30 % modulation depth
k_{DC}	Conversion gain of an envelope detector for a DC (low-frequency) input signal
K_{fD}	Technology dependent $1/f$ noise fitting parameter of a diode
K_{fR}	Technology dependent $1/f$ noise fitting parameter of a resistor
K_{fT}	Technology dependent $1/f$ noise fitting parameter of a transistor
K_{ij}	Residue of a partial fraction corresponding to real pole i with j -th degree denominator

K_{ILO}	Injection-locked oscillator gain
K_{mix}	Mixing gain of a mixer circuit
K_{VCO}	Integration constant or sensitivity of a VCO to its control voltage v_c
L	Inductance, an inductor
L	Length of a MOS transistor
$\mathcal{L}(\Delta\omega)$	Phase noise density at frequency offset $\Delta\omega$, relative to the carrier
L_{ij}	Residue of a partial fraction corresponding to complex pole i with j -th degree denominator
$\mathcal{L}_{total}(\Delta\omega)$	Total noise power density at frequency offset $\Delta\omega$, relative to the carrier
MoI	Moment of Impact of a pulse applied to a resonant tank
MoI_N	Moment of Impact of a pulse applied to a resonant tank, normalized to $T_{LC}/2$
N	Number of free-running periods in a Pulsed-Harmonic oscillator
NF_{amp}	Noise figure of an amplifier
N_{LF}	Noise spectral density of the low-frequency noise at an amplifier output (expressed in V^2/Hz)
$N_{o,ED}$	Noise spectral density of the noise at the output of an envelope detector (expressed in V^2/Hz)
N_{src}	Noise spectral density of an input source (expressed in V^2/Hz)
p	Frequency of a single pole
p_i	Real i -th pole frequency
$P(s)$	Numerator of a transfer function $H(s)$
P_s	Average power dissipated in a resonant tank
$P_{sbc}(\Delta\omega)$	Single-sideband noise power at offset frequency $\Delta\omega$, relative to the carrier
$\mathcal{P}_{side}(f_0 + \Delta f, 1 \text{ Hz})$	Single-sideband noise power in a 1 Hz interval at a frequency offset Δf from the carrier
PW	Pulse width of a pulse applied to a resonant tank
PW_N	Pulse width of a pulse applied to a resonant tank, normalized to $T_{LC}/2$
Q	Quality factor of a resonant (second order) network
q	Unit charge of a single charge carrier (electron or hole)
Q_C	Quality factor of a capacitor C
q_{Cte}	Maximum charge displacement (compared to equilibrium) in a resonant network with constant output amplitude during one period
q_{Decay}	Maximum charge displacement (compared to equilibrium) in a resonant network with exponentially decaying output amplitude during one period

Q_G	Generalized Q factor
Q_L	Quality factor of an inductor L
q_{max}	Maximum charge displacement from the equilibrium state on the output node of a resonant tank during one oscillation cycle
$Q(s)$	Denominator of a transfer function $H(s)$
R	Resistance, a resistor
r_0	Small signal output (drain) impedance of a MOS transistor (also called r_{ds})
R_B	Bulk resistance of a transistor
R_D	Drain resistance of a transistor
r_{ds}	Small signal output (drain) impedance of a MOS transistor (also called r_0)
R_{eff}	Effective noise resistance of a transistor
$\Re(x)$	The real part of x
R_G	Gate resistance of a transistor
R_p	Equivalent parallel resistance of an RLC network
R_S	Source resistance of a transistor
R_s	Series resistance of an inductor
s	Laplace variable, equal to $\sigma + j \cdot \omega$, in steady-state equal to $j \cdot \omega$
s	Second, unit of time
$S_{\phi,f}(f)$	Power Spectral Density of the phase fluctuations as a result of the $1/f$ noise component
$S_a(f)$	Power Spectral Density of a waveform a
$S_{i_n}(f)$	Power Spectral Density of a current noise source i_n
$S_{inj}(\omega)$	Power spectral density of the injected signal i_{inj}
$S_{nn}(\omega)$	Power spectral density of the free-running oscillator signal
$S_{osc}(\omega)$	Power spectral density of the locked oscillator signal i_{osc}
$S_{RF}(f)$	Power Spectral Density of a general RF signal
$S_{V_n}(f)$	Power Spectral Density of the voltage noise on a capacitor
$S_{v_n}(f)$	Power Spectral Density of a voltage noise source v_n
$S_x(f)$	Power Spectral Density of phase time fluctuations
$S_y(f)$	Power Spectral Density of fractional frequency fluctuations
$S_\phi(f)$	Power Spectral Density of phase fluctuations
$S_{\Delta f}(f)$	Power Spectral Density of frequency fluctuations
$S_{\Delta\omega}(f)$	Power Spectral Density of angular frequency fluctuations
T	Absolute temperature, expressed in Kelvin [K] or (depending on the context), the oscillation period
t	Time variable
T_0	Period of an oscillator
T_D	Delay of an oscillator stage
t_d	Delay of an inverter

T_h	Time span that a digital oscillator output is high during one period
$T_{h,0}$	Time span that a digital oscillator output is high during one period with a sensor input signal equal to zero
t_{hl}	Input-output delay of an amplifier for a falling edge at the output
$T_{i,reg}$	Loopgain of a current regulation circuit
T_l	Time span that a digital oscillator output is low during one period
t_L	Time needed for an injection-locked oscillator to lock, lock time of an injection-locked oscillator
$T_{l,0}$	Time span that a digital oscillator output is low during one period with a sensor input signal equal to zero
T_{LC}	Period of a free-running LC tank
t_{lh}	Input-output delay of an amplifier for a rising edge at the output
T_M	Motor torque
T_{Osc}	Complete period of a multi-stage oscillator
$T(s)$	Frequency dependent loopgain of a feedback system
T_{Sens}	Sensitivity of the output frequency f_0 to temperature
T_{Switch}	Time interval needed for a differential oscillator stage to switch
$T(t)$	Phase time
$T_{v,reg}$	Loopgain of a voltage regulation circuit
U	Symbol of electrical tension
\mathbf{u}_i	Eigenvector with corresponding eigenvalue λ_i
$u(t)$	The Heaviside function
V_A	Voltage amplitude over a capacitor
V_{bs}	Large-signal bulk-source voltage of a MOS transistor
v_{bs}	Small-signal bulk-source voltage of a MOS transistor
$v_c(t)$	Control voltage of a VCO
V_{Cte}	Constant input voltage
V_{ctrl}	Control voltage to control the gain of an amplifier
V_d	Differential voltage applied to the input of a differential pair
V_{dd}	Supply voltage
V_{ds}	Large-signal drain-source voltage of a MOS transistor
v_{ds}	Small-signal drain-source voltage of a MOS transistor
V_E	Early-voltage of a MOS transistor
V_{gs}	Large-signal gate-source voltage of a MOS transistor
v_{gs}	Small-signal gate-source voltage of a MOS transistor
$V_{gs,f}$	Zero-temperature-coefficient DC biasing voltage of a transistor
V_{gt}	Overdrive voltage of a MOS transistor, equal to $V_{gs} - V_{th}$
V_i	Output voltage of the i -th oscillator stage

$V_{i,reg}$	Regulated output voltage of a current regulation circuit
V_k	Fourier coefficient of a voltage oscillator signal
V_{max}	Maximum supply voltage at which a circuit can properly operate
v_{max}	Maximum output voltage (compared to equilibrium) of a resonant tank during one oscillation cycle
V_{min}	Minimum supply voltage at which a circuit can properly operate
$v_{n,diff}$	Differential noise voltage
$v_n(t)$	Small-signal noise voltage
V_{ref}	Output voltage of a voltage reference
V_{reg}	Output voltage of a voltage regulator
V_{rep}	Output biasing voltage coming from a replica circuit
$V(s)$	Laplace transform of a voltage waveform
V_S	Output voltage of a sensor, input voltage of a sensor interface
$V_{S,DC}$	DC value of the sensor output voltage
V_{Sens}	Sensitivity of the output frequency f_0 to the supply voltage
V_{S-}	Negative voltage output of a differential sensor
V_{S+}	Positive voltage output of a differential sensor
$v(t)$	Small-signal voltage
$v(t - \tau)$	Decay function of the excess amplitude
V_T	Threshold voltage of a relaxation oscillator
V_t	Thermal voltage, equal to $k \cdot T/q = 26$ mV at room temperature
V_{th}	Threshold voltage of a MOS transistor
V	Volt, unit of electrical tension
$V_{v,reg}$	Regulated output voltage of a voltage regulation circuit
$V_{v,reg,rep}$	Regulated output voltage over the oscillator replica when the regulator is loaded with a resistor
$V_{v,reg,res}$	Regulated output voltage of a voltage regulation circuit loaded with a resistor
W	Width of a MOS transistor
x	Normalized variable of the ISF $\Gamma(x)$, typically equal to $\omega_n \cdot t$
\dot{x}_i	Time-derivative of x_i
$x_i(t)$	A real-valued function of t
$x(t)$	Random instantaneous phase time variation, $\phi(t)/\omega_0$
$y(t)$	Instantaneous fractional frequency variation, $dx(t)/dt$
Z	Complex impedance
z	Scalar for which $z \in \mathbb{Z}$
Z_k	Impedance of a resonant network, seen by the k -th harmonic

Figures

Fig. 1.1	a Schematic drawing of <i>The Thing</i> . The working principle is based on the reflection of an RF signal by the antenna. The load impedance of the antenna is changing as a function of the sound pressure. b <i>The Thing</i> was hidden in a replica of the Great Seal [292]	2
Fig. 1.2	a Schematic drawing on the electromagnetic rotation experiment or homopolar motor. b Schematic drawing of an induction experiment [304].	4
Fig. 1.3	James Clerk Maxwell proved mathematically that the rings of Saturn consist of numerous small particles [315].	5
Fig. 1.4	Nikola Tesla aged 36 [291] and two of his patents, one for the efficient generation of RF power, a second for his Tesla transformer [248, 249].	6
Fig. 1.5	a Photograph of Marconi’s Magnetic Detector. b Schematic drawing of the Magnetic Detector [237, 302]	7
Fig. 1.6	Photograph of a crystal detector or cat’s whisker. The metal-semiconductor junction which was created is nowadays known as a Schottky diode [287]	8
Fig. 1.7	The RMS Titanic was believed to be unsinkable [308]	9
Fig. 1.8	Schematic of the autodyne or regenerative receiver. The photo <i>on the right</i> shows the simplicity of this circuit [307]. . .	10
Fig. 1.9	Idealized cross-section of an <i>n</i> -channel (<i>left</i>) and <i>p</i> -channel (<i>right</i>) JFET. By reversely biasing the <i>pn</i> junction at the gate, the conducting channel is pinched off [97].	11
Fig. 1.10	Cross section of a typical <i>npn</i> (<i>left</i>) and <i>pnp</i> (<i>right</i>) transistor structure.	12
Fig. 1.11	Cross-section of an NMOS (<i>left</i>) and PMOS (<i>right</i>) transistor. Even in unbiased condition a depletion region is present surrounding the source and drain doping implant . . .	14

Fig. 1.12 One of the illustrations of Kilby’s patent No. 3261081. This device is considered to be the first integrated circuit [130] 15

Fig. 1.13 Logarithmic plot of the number of calculations per second per \$1,000. From the early beginning, this curve increases exponentially [233] 16

Fig. 1.14 System overview of the three hierarchical layers in the Pinballs platform. 19

Fig. 1.15 Typical charge and discharge characteristic of the supply curve on an RFID tag. Most often the scavenging mechanism is rather slow, which results in a T_{charge} in the order of minutes. Depending on the load current and the size of the capacitor, T_{act} typically varies between 1 ms and several seconds. The higher V_{max} and the lower V_{min} , the longer the tag circuitry can be active without interruptions (one burst operation). 22

Fig. 1.16 Architecture of a wireless RF-powered tag 23

Fig. 2.1 The graphical representation of the 1-dimensional phase space gives a good insight in the first-order system’s behavior. All the possible states of the system are represented by unique points on the *horizontal axis*. The *vertical axis* is only added for better understanding. 33

Fig. 2.2 Phase portraits of different linear second-order systems with **a** two positive eigenvalues, **b** a positive and a negative eigenvalue, **c** two negative eigenvalues. **a** and **b** are both called unstable systems, **c** is a stable system. 35

Fig. 2.3 Phase portraits of different linear second-order systems with two complex conjugate eigenvalues. The real part has **a** a positive sign, **b** a value equal to zero, **c** a negative real part. **a** is called an unstable system, **b** is marginally stable and **c** is a stable system 37

Fig. 2.4 Phase portraits and output signal of the van der Pol oscillator for different values of μ . The initial value for the *blue curve* is (0.01, 0.01), for the *green curve* this is (3, 3). On each phase portrait the 50 *blue circles* are equidistant in time to show the behavior of the oscillator during the limit cycle. **a** $\mu = 0.1$, **b** $\mu = 0.5$, **c** $\mu = 5$, **d** $\mu = 20$ 38

Fig. 2.5 Behavior of the van der Pol oscillator with a PI amplitude regulator, $A = 1/\sqrt{2}$, $\mu = 0.05$ and $\eta = 0.01$. **a** Shows the behavior in the time domain. The output signal $x_1(t)$ is shown *on the left*. *On the right* $x_3(t)$ is plotted, which corresponds to the resulting output signal of the amplitude regulator. **b** Shows the behavior in the phase plane/space; the overshoot of the amplitude is clearly visible. It takes a lot of periods before the limit cycle (*on the right*) is reached. 41

Fig. 2.6 Chaotic behavior of the forced modified van der Pol equation. The *circles* show the evolution of 32 near start conditions over time. The *blue line* is an $x_1 - x_2$ plot of one of the trajectories 42

Fig. 2.7 Two coupled energy tanks, an inductor L and a capacitor C , forming an oscillator 44

Fig. 2.8 An inductor can exchange its energy with a kinetic energy tank. A DC motor is needed to do the energy conversion. 46

Fig. 2.9 Different RLC tanks. The *left* tank (a) is not driven and its losses are represented by the parallel resistor. In (b) the same tank is driven by a transconductance amplifier. In (c) the losses are represented by a series resistor in the inductor, which is the closest to the real situation. 53

Fig. 2.10 Different definitions of the Q factor of a two-pole system, based on the width (bandwidth) of the resonant peak and based on the steepness of the phase shift of the feedback network 55

Fig. 3.1 Phase noise spectrum at the output of a generic oscillator. According to the power-law noise model, the spectrum can be divided in different zones, with a different noise origin or underlying mechanism. 65

Fig. 3.2 The noise theory of Leeson-Cutler is based on the idea that the injected noise is multiplied by the transfer characteristic of the resonant network. Although this is an explanation for the $1/f^2$ slope in the phase noise spectrum, it does not take the up-conversion of the injected $1/f$ noise into account 67

Fig. 3.3 The response of an oscillator to an injected noise current can be modeled using two single-input, single-output systems, one for the excess phase and one for the instantaneous amplitude. 69

Fig. 3.4 State diagram of a free running LC tank. The losses in the tank result in a decreasing oscillation. It is clear that the sensitivity to an injected noise pulse does not only depend on the moment of impact, but also on the amplitude 69

Fig. 3.5 An injected signal with amplitude I_n is converted to the spectrum of the excess phase $\phi(t)$. The signal is weighted by the Fourier coefficients of the ISF $\Gamma(x)$. Furthermore, a low-pass filtering is applied by the integral, in this way the signals close to the carrier or to one of the harmonics are dominant on the signals further away. The second step is the phase modulation of this excess phase. During this operation, the injected signal is up-converted to the carrier frequency (and to its harmonics) 71

Fig. 3.6	Similar to Fig. 3.5, this figure shows the translation of a noise spectrum towards the oscillator phase noise spectrum. During the convolution of the ISF and the injected noise, the noise contribution around each harmonic of the ISF is translated into noise around zero in the spectrum of the excess phase $\phi(t)$. Keep in mind, however, that the noise contributions appear around each of the ISF harmonics but are filtered by the integral operator. During the phase modulation step, the spectrum is up-converted towards the oscillator center frequency and the harmonics. Although the LTV theory of Hajimiri predicts an infinite noise power close to the carrier, a Lorentzian spectrum is drawn.	73
Fig. 4.1	Typical block diagram of a harmonic (linear) oscillator	93
Fig. 4.2	A parallel RLC network, as shown previously in Fig. 2.9a.	98
Fig. 4.3	Two typical structures of an integrated inductor. <i>Above</i> an electronic model is shown with some of the parasitics. Note that the number of components in the lumped inductor model needed to accurately simulate the behavior, depends on the wavelength of the applied signal. Due to its small dimensions (usually smaller than 1 mm), and the lossy silicon substrate underneath, a lot of capacitive parasitics arise. Furthermore, the series resistance and Eddy currents in the substrate cause significant energy losses.	104
Fig. 4.4	Schematic drawing of the losses in an inductor, both caused by the flow of a changing current in the conductor. a Eddy currents are circular currents in the substrate, which cause a power loss and a decrease of the inductance. b Skin effect: due to circular currents in the conductor itself, the current is forced to the outer shell of the conductor.	105
Fig. 4.5	Comparison between different communication technologies: the bandwidth BW is plotted versus the maximum frequency error.	111
Fig. 4.6	Qualitative comparison of different properties of (uncompensated) crystal oscillators and silicon replacement circuits [176]. The <i>dashed green line</i> shows that a huge benefit of cost and size can be achieved when the oscillator can be integrated together with all other CMOS circuitry	112
Fig. 4.7	Block schematic of a generic harmonic oscillator. a A single-ended amplifier and a feedback network. b Its differential equivalent. The amplifier compensates for the losses in the feedback network	113

Fig. 4.8 Typical differential implementation of an LC oscillator. *On the left*, the amplifier is implemented with NMOS transistors; *on the right* PMOS transistors are used. A combination of both is also possible [212] 115

Fig. 4.9 A quadrature oscillator is forced towards its zero temperature frequency by cross-injection of quadrature signals [109]. The amplitude control is used to keep the amplifiers in the linear region. An external trimming circuit is used to trim g_{mc} towards the T-null frequency 116

Fig. 4.10 Low-noise differential Colpitts topology presented in [252]. Because of their better noise performance, only PMOS transistors are used 117

Fig. 4.11 Differential LC topology with an altered cross-coupling of the active devices [117] 118

Fig. 4.12 Tunable RC oscillator based on a single current conveyor [116] 119

Fig. 4.13 Schematic drawing of a commonly used RC feedback network, called Wien bridge. *On the right* also its dual RL equivalent is shown. 120

Fig. 4.14 Transfer function of the Wien bridge feedback network 120

Fig. 4.15 Schematic of the Wien bridge, which was used, similar to the Wheatstone bridge, to measure the value of capacitors in terms of frequency and resistance 122

Fig. 4.16 Schematic drawing of an astable multivibrator. *On the right* the output waveforms are shown. 123

Fig. 4.17 Schematic drawing of a relaxation oscillator based on a multivibrator [192]. *On the right* the output waveforms are shown. The reference voltage is equal to 1 V and the latch has a delay of 50 ms 123

Fig. 4.18 The noise on the reference signal is directly translated to timing jitter on the next charging curve 125

Fig. 4.19 Schematic of a low-jitter relaxation oscillator. The frequency is determined by C_2 , I_1 and the value of V_{c2} at which the current through M_1 is equal to I_1 , called $V_{ref,2}$. *On the right* the output waveforms of a simulated Matlab model are shown. The output signal V_{out} is obtained by putting V_{c1} through a comparator. As can be seen, $V_{ref,1}$ (*dashed line*) has no impact on the timing of the rising edges in the output signal 126

Fig. 4.20 Block diagram of a 3-stage ring oscillator 127

Fig. 4.21 Schematic of a fully-differential delay stage with a symmetrical load as used in [244]. The delay can be controlled through V_{ctrl} 128

Fig. 4.22	Schematic of a mobility-based current source. The current I_0 is based on an externally applied reference voltage V_R	130
Fig. 4.23	Schematic of a mobility-based current source. By controlling the inversion level of M_{n1} , the output current I_B can be made PTAT	131
Fig. 4.24	Schematic drawing of an ETF. The heater (H) is driven with a square wave: the heat transfers through the silicon to the temperature sensors (S) which are laid out in circular pattern around the heater	132
Fig. 4.25	Schematic drawing of an FLL using an ETF. The VCO locks on the thermal delay of the ETF, resulting in $\phi_{ETF} = \phi_{ref}$	133
Fig. 4.26	Qualitative comparison of different integrated oscillator topologies from literature	134
Fig. 5.1	Conventional Wien bridge topology using a passive feedback network and an opamp. Due to the feedback resistors, the amplifier has a gain of 3	140
Fig. 5.2	Schematic and small-signal model of a common-source amplifier with drain resistor	142
Fig. 5.3	Small-signal model of the improved Wien bridge oscillator Topology	143
Fig. 5.4	Complete amplifier used in the Wien bridge oscillator	144
Fig. 5.5	Gain-boosting amplifier for the lower cascode transistors	145
Fig. 5.6	Bode plot showing the gain of the gain-boosting amplifiers and the complete amplifier. The source impedance of the cascode transistors is also shown. The <i>dashed lines</i> indicate the active region of the gain boosters.	145
Fig. 5.7	Schematic of the amplitude-regulator circuit	147
Fig. 5.8	Gain of the amplifier as a function of the voltage applied to the bridge transistor.	148
Fig. 5.9	Complete schematic of the Wien bridge oscillator. The gain-boosting amplifiers and the amplitude-regulator circuit are omitted for clarity reasons	149
Fig. 5.10	Main noise sources in the transconductance amplifier	150
Fig. 5.11	Small-signal schematic of the differential oscillator. The noise contributions of the amplifier are grouped in $i_{n,A}^2$. Note that $v_{out} = v_1 - v_3$	151
Fig. 5.12	Bode plot of the noise transfer functions. The sharp peak is the resonance frequency of the closed-loop system	152
Fig. 5.13	Small-signal schematic of a single-ended Wien bridge oscillator. The propagation of the amplifier noise to the output is proven to be the same as in the differential case. Note that $v_{out} = v_1$	152

Fig. 5.14 ISF of the Wien bridge oscillator, normalized to the maximum output voltage v_{max} . Two *curves* are shown, one for the input node and one for the output node of the feedback amplifier. In the *lower graph*, the output waveform of the oscillator is shown 153

Fig. 5.15 Chip photomicrograph of the implemented Wien bridge oscillator 155

Fig. 5.16 Measured frequency deviation as a function of temperature for different samples. The frequency was normalized at 20 °C; some samples did not work at 120 °C. 156

Fig. 5.17 Measured phase noise as a function of the carrier frequency offset for 3 different samples 156

Fig. 5.18 An LDO regulator typically consists of a voltage reference, an output transistor and a feedback amplifier 160

Fig. 5.19 The used Wien bridge oscillator. The resistors in the feedback network are implemented by the output impedance of the amplifiers. $V_{v,reg}$ and $V_{i,reg}$ are biasing voltages, both delivered by the regulator circuitry. 161

Fig. 5.20 The two oscillators are coupled in opposite phase by the coupling capacitors C_c . Note that the current sources of the differentially oscillating amplifiers are shared to draw a constant current over time. The biasing voltage V_{rep} is delivered by an amplifier replica; $V_{v,reg}$ and $V_{i,reg}$ are biasing voltages, both delivered by the regulator circuitry 162

Fig. 5.21 The voltage regulator is based on the V_{th} -based voltage reference *on the left*. The output voltage is determined by the threshold voltages of M_1 and M_2 164

Fig. 5.22 Two regulators are used to provide a stable output voltage and current to the oscillator. The current regulator is directly connected to a replica of the amplifier used in the oscillator. The output current of the regulator only changes 0.02 % over a 1 V voltage drop. 165

Fig. 5.23 Simulated output of the voltage and current regulator. The relative deviation compared to the output voltage at 1 V is shown. In the *lower graph* also the relative output frequency variation as a function of the supply voltage is shown 166

Fig. 5.24 Simulated loop gain of the regulators ($T_{v,reg}$ and $T_{i,reg}$) and the power supply rejection ratio (PSRR) at the output of the oscillator. The supply voltage is 1.0 V. The current and voltage regulator have a phase margin of 70° and 58° respectively 166

Fig. 5.25 Simulated output deviation of the regulators as a function of temperature. The *upper graph* shows the output voltage of the regulators. In the *lower graph*, the output current and the resulting oscillator frequency are shown. 167

Fig. 5.26 Simulated output deviation of the regulators as a function of temperature when a resistor is used as the reference load of the current regulator. The *upper graph* shows the output voltage of the regulators and the voltage over the replica. In the *lower graph*, the output current through the oscillator replica and the resulting oscillator frequency are shown. 168

Fig. 5.27 Chip photomicrograph of the proposed voltage-independent oscillator; the active area measures 200 $\mu\text{m} \times 150 \mu\text{m}$ 169

Fig. 5.28 The layout of the oscillator core is built completely point-symmetrically. Every current is flowing in four directions to reduce the systematic influence of the silicon crystal and other non-isotropic influences. 169

Fig. 5.29 Relative frequency deviation of the measured oscillator samples. *On the right*, the oscillation frequency of each sample at 1 V is reported. The maximum frequency variation is 104 ppm over the 0.4–1.4 V supply voltage span 170

Fig. 6.1 Block diagram of a pulsed-harmonic oscillator. Instead of a negative resistance or g_m , only an NMOS switch is used to drive the tank. PG is the pulse generator 174

Fig. 6.2 Simulated output waveform of a pulsed LC oscillator. Between pulses the amplitude is decaying due to the losses in the LC tank 175

Fig. 6.3 Some of the possibilities to build a tuned network. RC and LC networks are commonly used in fully integrated oscillator implementations. Crystals can only be used as an external component 175

Fig. 6.4 A crystal can be modeled by a series LRC circuit with a capacitor in parallel [219]. This parallel capacitor C_p is mainly caused by the parasitics of the casing 176

Fig. 6.5 When drawing the magnitude of a transfer function in the complex plane, it is seen that the Bode plot is the cross-section of this surface with the (*positive*) imaginary axis. Therefore, a Bode plot only shows the steady-state response of a system 179

Fig. 6.6 Phasor diagram of the impulse response. To keep the period constant, a new Dirac impulse must be applied at the zero crossing of the cosine and *not* at the maximum of $h(t)$ 184

Fig. 6.7 Schematic model of the tank. This model is numerically simulated in Matlab; the switch is closed (*pulsed*) once every n cycles. 184

Fig. 6.8 Illustration of PW and MoI compared to the tank output waveform. 185

Fig. 6.9 Impact of a real pulse applied to the network of Fig. 6.7. When the right combination of pulse width (PW) and moment of impact (MoI) are applied (indicated by the *black line*), the time between the zero crossings is not biased. All the values are normalized to half the LC tank oscillation period. 185

Fig. 6.10 Oscillation amplitude as a function of the pulse width (PW) and the moment of impact (MoI). A longer pulse leads to a higher amplitude, but also the moment of impact has a small influence on the output amplitude of the tank. All the values are normalized to half the LC tank oscillation period. 185

Fig. 6.11 Optimal width ($\Delta T = 0$) of the applied pulses (PW) as a function of the moment of impact (MoI) for different switch resistances R_p . Both axes are normalized to $T_{LC}/2$, half the LC tank oscillation period 186

Fig. 6.12 Sensitivity of the oscillation period to the moment of impact. The derivative is calculated for the optimal PW-MoI combinations. All axes are normalized to half the oscillation period since this is the time span in which the pulse is applied. 187

Fig. 6.13 Sensitivity of the oscillation period to the pulse width. The derivative is calculated for the optimal PW-MoI combinations. All axes are normalized to half the oscillation period since this is the time span in which the pulse is applied. 187

Fig. 6.14 Phase portrait of a pulsed oscillator. The LC network is similar to Fig. 6.7 with a switch discharging the state capacitor. An equal noise voltage ΔV is added at two different moments in the oscillation, causing a different phase shift $\Delta\theta$ in the output wave 190

Fig. 6.15 *Top* The ISF of the pulsed oscillator. The *blue curve* is the numerically simulated ISF; the *red dashed curve* represents the analytically calculated ISF during the free-running period. Both curves are almost identical. *Bottom* The corresponding output waveform of the LC tank. The *red dashed line* shows the pulses applied to the LC tank 193

Fig. 6.16 Fast Fourier transform of the ISF. The most important frequency component is at $32 \cdot f_0 = f_{LC}$ 195

Fig. 6.17 The amplifier used to detect the LC output signal is a differential pair in combination with 2 differentially biased CMOS inverters. The differential pair is shown (*right*) together with the supply-independent biasing circuit (*left*) [188] 198

Fig. 6.18 Delay and peak-to-peak output signal of the amplifier for different input amplitudes at $V_{dd} = 1.1$ V and for a falling and a rising edge at the input. The circuit is able to detect a 10 mV signal when the biasing current is 10 μ A. When the current is decreased, the sensitivity also decreases. 199

Fig. 6.19 The ripple counter is built out of 5 modified TSPC flip-flops 199

Fig. 6.20 The pulse width of the pulse generator is controlled by the inverter delay in combination with the output capacitor 200

Fig. 6.21 Impact of the changing temperature on the output PW and MoI. The combined impact on the pulsed period is also shown 201

Fig. 6.22 Photomicrograph of a pulsed LC oscillator. Some other unrelated test circuitry is laid out under the inductor. The chip area is 1,750 μ m by 1,500 μ m. 203

Fig. 6.23 Measured relative frequency error of the twelve measured samples. As predicted in Sect. 6.6.4.1, the frequency drops with increasing temperature 203

Fig. 6.24 Measured relative frequency error over different supply voltages of the twelve samples 204

Fig. 6.25 Output jitter of the oscillator. The *upper plot* shows the simulated jitter, without supply noise. In the *second plot*, supply noise is added to simulate the noise injection of the digital circuitry as well as thermal noise to match the measured output jitter, which is shown in the *third plot*. The last plot shows the jitter on only the odd periods, since this is a more correct representation of the random (accumulated) noise in the system 205

Fig. 7.1 System overview of the wireless sensor network (WSN) with RF clock distribution. The specifications of the clock carrier in terms of temperature and supply voltage stability are unimportant as long as the different network components can lock to the carrier 210

Fig. 7.2 Generic model of an oscillator, $H(s)$ is the tuned feedback network and $G(s)$ represents the amplifier. When a small current i_{inj} is injected, a phase shift is caused at the input of the feedback network. 211

Fig. 7.3 Amplitude and phase of the generic transfer function of the oscillator. The angular frequency is normalized to ω_n and the amplifier needs a gain of 4 to obtain a stable oscillation. A frequency shift causes a nonzero phase shift in the feedback network 211

Fig. 7.4 Phasor diagram of the different currents in locked condition. *On the left*, the oscillator current i_{osc} leads the injected current i_{inj} , introducing a positive phase shift ($\omega_i < \omega_n$). *On the right*, i_{osc} lags i_{inj} , introducing a negative phase shift ($\omega_i > \omega_n$). 212

Fig. 7.5 Schematic of a relaxation oscillator using a Schmitt trigger. The current sources are switched on and off by the output signal of the Schmitt trigger. This results in a *triangular* output waveform V_C 213

Fig. 7.6 Waveforms in the relaxation oscillator. V_C is the voltage on the capacitor while I_C is the current from the current sources. All waveforms are scaled to be able to denote the necessary time parameters. 214

Fig. 7.7 Pull-in time for an injection-locked oscillator as a function of the initial angle $\phi_{i,0}$ and the steady state angle ϕ_∞ . The time, normalized to $1/\omega_L$, to enter the interval $\phi_\infty - 0.01 < \phi_i(t) < \phi_\infty + 0.01$ is shown since the actual pull-in process occurs exponentially 220

Fig. 7.8 Normalized beating frequency as a function of the normalized offset frequency. The influence of the injected signal is the largest when approaching the lock range. At the borders of the lock range, the beating frequency is equal to zero 221

Fig. 7.9 Phase difference between the injected signal and the oscillator output when the injected signal is just out of the lock range ($\omega_L = 1$). The frequency difference between the injected signal and the oscillator output is also shown. When the phase shift is around 90° (-90°), the influence is the highest and the oscillator output ‘tries to follow’ the injected signal. From the moment the phase shift increases (decreases) further, the oscillator frequency falls back until the next clock edge arrives. The nominal oscillator frequency, ω_n , is also shown in the graph 222

Fig. 7.10 One-port representation of an oscillator. The negative G_m is slightly nonlinear to implement an amplitude control mechanism 223

Fig. 7.11 Block diagram of a first order PLL, used to model an injection-locked oscillator. 227

Fig. 7.12 Transfer characteristic for both the oscillator noise (*top*) and the noise on the injected signal (*bottom*). When the frequency difference $\Delta\omega_n$ between the natural oscillator frequency and the injected signal increases, the -3 dB filter frequency $K_{ILO}(\phi_\infty)$ decreases. 228

Fig. 7.13 Normalized -3 dB frequency of the filter characteristic as a function of the normalized frequency difference between the natural oscillator signal and the injected signal $\Delta\omega_n$. The different *curves* are for different injection levels and are all normalized to their corresponding lock range ω_L 228

Fig. 7.14 Example noise spectrum of an injection-locked oscillator as a function of the injected noise spectrum S_{inj} and the oscillator spectrum S_{nm} for different values of ϕ_∞ . The spectrum within the lock range is mainly determined by the injected spectrum and the oscillator noise at the edge of the lock range. The frequency is normalized to ω_n and $\omega_L = 0.1$ 229

Fig. 7.15 Block diagram of the injection-locked oscillator system. After buffering the antenna signal, it is injected to the differential oscillator which acts as a 2-fold frequency divider. Also a phase detector is implemented to detect a lock condition or to further increase the lock range 230

Fig. 7.16 Schematic of the two-stage RC feedback network, based on a Wien bridge oscillator 230

Fig. 7.17 Schematic of the differential implementation of the proposed oscillator. By connecting the 2 oscillators differentially and by sharing the capacitor in the first stage, the oscillators are forced in opposite phase. The voltages v_{s1} and v_{s2} are used to implement a lock detection circuit and a circuit to increase the lock range. 231

Fig. 7.18 The injection-locked oscillator can be described as a single balanced mixer. *On the left* the current with angular frequency $2 \cdot \omega_i$ is injected at the sources of the differential pair. This corresponds to the current source *on the right* with angular frequency ω_i . K_{mix} is the conversion gain of the mixer 233

Fig. 7.19 Average output frequency and phase difference as a function of the frequency of the injected signal. The phase curves can be obtained by mixing the oscillator signal (or a 90° -shifted version) with the injected signal 234

Fig. 7.20 Schematic of the integrating phase detector. The biasing of the detector is done by the differential stage *on the right*, making use of the common-mode signal coming from the oscillator biasing replica. The detector has two inputs: the antenna signal coming from the output of the first stage of the input amplifier and the common-mode source voltage of one of the two oscillator stages, v_{s1} or v_{s2} . **a** Shows a single-ended version with a digital output; **b** is a differential implementation with a lower gain and an analog output. 235

Fig. 7.21 Measured free-running frequency of 3 different samples. Also the minimum upper bound and maximum lower bound of the lock range of all 8 samples are shown as a function of **a** the temperature and **b** the supply voltage 237

Fig. 7.22 Photomicrograph of the injection-locked oscillator. 238

Fig. 7.23 Block diagram of the clock and receiver circuitry. Only the input amplifier and the AM demodulator are working at the (high) carrier frequency 239

Fig. 7.24 System overview of the wireless sensor network (*WSN*) with RF clock distribution and coordination receiver. The specifications of the clock carrier in terms of temperature and supply voltage stability are unimportant as long as the different network components can lock to the wirelessly distributed clock signal. The implemented downlink makes network coordination possible and avoids data collisions 239

Fig. 7.25 Schematic of the differential implementation of the proposed oscillator. By connecting the 2 oscillators in series, both transistor branches are oscillating differentially 240

Fig. 7.26 Schematic of the first and third stage of the four-stage input amplifier. Each stage has its own common-mode feedback, implemented by the two NMOS transistors on *top*. The first stage also has two biasing resistors to set the DC level of the antenna inputs. The input is AC-coupled and the third stage contains a DC-suppression capacitor 241

Fig. 7.27 Bode plot of the 4-stage front-end amplifier stages. The gain of the first stage at 2.4 GHz is around 15 dB or 6. The total gain is between 6 and 720, depending on the number of stages 241

Fig. 7.28 AM-detector with an NMOS input pair. In practice, two AM-detectors, NMOS and PMOS, are used to generate a differential signal which can be injected differentially into the oscillator. 242

Fig. 7.29 Conversion gain of the envelope detectors for different input levels. *On the left*, the conversion gain is shown as a function of the input amplitude with 30 % modulation depth. Note that this is the simulated output amplitude divided by the carrier amplitude and not the amplitude of the envelope. *On the right*, the same graph is shown for a signal with 100 % modulation depth 243

Fig. 7.30 The output of both AM detectors is combined in a differential amplifier before injecting it into the oscillator. The gain of the amplifier can be controlled by adapting V_{ctrl} . The AM signal is also amplified by a two-stage amplifier to obtain a digital signal at the input of the phase detector. 244

Fig. 7.31 Bode plot of the two baseband amplifiers including the high-pass filter at the input. The first amplifier, which amplifies the baseband signal towards the oscillator, has a controllable gain. This is shown in the graph *on the right* (simulated for a 1 V supply voltage, at 30 MHz) 244

Fig. 7.32 Detailed overview of the receiver chain. The operations performed on the input spectrum are schematically drawn *at the bottom*. The combination of two phase detectors detects the negative envelope as well as the positive envelope of the input waveform, which results in a signal gain of 2 245

Fig. 7.33 The hockey stick curves show the input referred noise of the AM receiver chain for different input resistances and a 30 % modulation depth. The crossing of these curves with the $P_{in} - SNR_{min}$ curve determines the minimum detectable input signal level. *On the left* the input gain is equal to 6 (1 stage), *on the right* an input gain of 30 is assumed (2 stages) 246

Fig. 7.34 The hockey stick curves show the input referred noise of the AM receiver chain for different input resistances and a 100 % modulation depth. The crossing of these curves with the $P_{in} - SNR_{min}$ curve determines the minimum detectable input signal level. *On the left* the input gain is equal to 6 (1 stage), *on the right* an input gain of 30 is assumed (2 stages) 246

Fig. 7.35 The receiver consists of a simple shift register of which the first flipflop is used as a phase detector. When a phase shift is applied to the input, the data register will clock. Depending on the most significant bit of the counter, which counts the clock cycles between two phase shifts, a zero or a one is received. In the subsequent clock cycle, the counter is reset . . . 248

Fig. 7.36 The simulated waveforms of an injection-locked receiver. Three times a 180° phase shift is applied to the injected signal. The *bottom graph* shows the evolution of the phase difference. It takes around 10 periods until the output of the phase detector recovers from the phase shift. Note that the oscillator only has a weak nonlinearity in its amplifier, which results in a slow amplitude regulation 249

Fig. 7.37 Photomicrograph of the 40 nm injection-locked oscillator and receiver 251

Fig. 7.38 Measured free-running frequency of 3 different samples of the 40 nm implementation. Also the estimated lock range is shown as a function of **a** temperature and **b** supply voltage . . . 252

Fig. 7.39 Operating range of the injection-locked receiver and the upper and lower limit of the lock range without controlling the baseband gain. *On the left* an input gain of 6 is used, *on the right* the input gain is equal to 30 253

Fig. 7.40 Operating range of the injection-locked receiver and the upper and lower limit of the lock range with baseband gain control. V_{ctrl} was set to 0.75 V (or $V_{dd} - 0.25$ V). *On the left* an input gain of 6 is used, *on the right* the input gain is equal to 30 253

Fig. 8.1 Block diagram of a PLL-based sensor interface. The resistors R_s represent the sensor input, which is connected to an oscillator. Due to the phase detector and the digitally controlled feedback resistors R_v , both oscillator frequencies are matched 258

Fig. 8.2 Block diagram of the PWM-based sensor interface. Half of the oscillator stages are slowed down by the sensor signal, the other half is sped up. The output latch converts the oscillator signals into a PWM signal of which the duty cycle is proportional to the sensor value. 260

Fig. 8.3 Schematic of two oscillator stages and their interconnection. When a rising edge is applied to the input, the capacitor charges linearly and activates the next stage. The oscillator stage is reset by the output signal of stage $n + 3$. In this way, all internal control signals are generated by the oscillator itself 261

Fig. 8.4 Sketch of the output waveforms of subsequent oscillator stages. When using a CMOS differential pair, the switching delay when applying a linearly increasing input is exactly the same as in the case of an amplifier with an infinite gain. This is due to the point-symmetry of the differential pair 262

Fig. 8.5 Transfer characteristic of a differential oscillator stage. The characteristic is point-symmetric around $V_d = 0$. The linearized characteristic is shown as a *dashed line*. 262

Fig. 8.6 Two configurations of a Wheatstone bridge: one with a current source on *top*, the other connected to an input voltage source 263

Fig. 8.7 The sampling of the oscillator output signal when the duty cycle is equal to 1/3. If only the *black samples* are taken into account, the samples need to be averaged over several periods. However, when the sampling speed is higher (*all samples*), only the first period is enough to obtain the right duty cycle. This shows the trade-off between the sampling speed and the bandwidth 265

Fig. 8.8 Simplified schematic of the different noise contributions: **a** noise in the reference voltage V_S ; **b** noise in the differential pair; **c** noise in the current source 266

Fig. 8.9 The jitter on the complete oscillator period ($T_{l,0} + T_{h,0}$) as well as the jitter on half the oscillation period ($T_{l,0}$ or $T_{h,0}$) are present in the interface’s output signal 273

Fig. 8.10 Normalized jitter (compared to the noise for a zero-input signal) of the output duty cycle as a function of the varying sensor input. The *solid line* uses a differential sensor; the *dashed line* is for a single-ended sensor. The noise sources themselves are constant; the variation is caused by the input–output transfer characteristic of the noise 275

Fig. 8.11 The normalized jitter (compared to the noise for a zero-input signal) of the output duty cycle as a function of the varying sensor input for the noise generated by the current source. The variance of the noise increases linearly with the stage delay. The *solid line* uses a differential sensor; the *dashed line* is for a single-ended sensor 276

Fig. 8.12 The most important design parameters of the PWM-based sensor interface in 130 nm CMOS 279

Fig. 8.13 Output waveform of 4 oscillator stages. The linear charging curve as well as the slow switching and the point-symmetry of the switching operation are clearly visible 280

Fig. 8.14 Linearity error of the output duty cycle as a function of the input voltage. In **a** the supply voltage V_{dd} is varied from 0.9 to 1.6 V; in **b** the temperature is varied from -40 to 120°C 281

Fig. 8.15 Simulated error on the output duty cycle as a function of the input resistance. In **a** V_{dd} is varied and the error is relative to the output value at 1.2 V. In **b** the temperature is varied (-40 to 120°C), the error values are relative to the output value at 30°C . The maximum error appears at low temperatures for high input values and is equal to 1.2 % 281

Fig. 8.16 Output spectrum of the sensor interface in 130 nm. The noise bandwidth is equal to 1 MHz, the 100 kHz, 25 % amplitude input signal is clearly visible 282

Fig. 8.17 The SNR and SNDR as a function of the input amplitude. From the SNDR also the ENOB can be calculated. A maximum is reached for an input amplitude between 10 % and 25 % of $V_{S,DC}$ 282

Fig. 8.18 The most important design parameters of the PWM-based sensor interface in 40 nm CMOS 283

Fig. 8.19 Simulated output waveform of the 40 nm oscillator at a supply voltage of 1.2 V. When the output of stage 7 ($n + 3$) is active, the current of stage 4 (n) can be switched off 284

Fig. 8.20 Schematic of the current switch circuit. The current source is switched off when the stage is reset. When the oscillator is not oscillating, all current sources are switched on, which enables the startup of the oscillator 285

Fig. 8.21 Linearity error of the output duty cycle as a function of the input sensor resistance. In figure **a**, the supply voltage V_{dd} is varied from 0.6 to 1.6 V. In figure **b** the temperature is varied from -40 to 120°C 286

Fig. 8.22 Error of the output duty cycle as a function of the input sensor resistance. In **a** V_{dd} is varied and the error is relative to the output value at 1 V. At all supply voltages (0.9 to 1.6 V) the error stays *below* 0.5 %. In **b** the temperature is varied (-40 to 120°C), the error values are relative to the output value at 70°C . The maximum error appears at high temperatures for high input values and is around 1.1 % 286

Fig. 8.23 Linearity error of the output duty cycle as a function of the input sensor voltage. In figure **a** the supply voltage V_{dd} is varied from 0.6 to 1.6 V. In **b** the temperature is varied from -40 to 120°C 287

Fig. 8.24 Error on the output duty cycle as a function of the input sensor voltage. In **a** V_{dd} is varied and the error is relative to the output value at 1 V. At all supply voltages (0.9 to 1.6 V) the error stays *below* 0.5 %. In **b** the temperature is varied (-40 to 120°C) and the error values are relative to the output value at 30°C . The maximum error appears at high temperatures for high input values and is around 1.5 % 287

Fig. 8.25 The SNR and SNDR as a function of the input amplitude. From the SNDR also the ENOB can be calculated. The maximum in this case is reached at lower input amplitudes due to the increased nonlinearity. 288

Fig. 8.26 The static nonlinearity of the sensor interface. In the *upper graph*, the nonlinearity is shown for a differential ± 180 mV input signal. The *graph below* shows the nonlinearity for a smaller input range of ± 140 mV. The nonlinearity slightly decreases when the supply voltage increases. 289

Fig. 8.27 Photomicrograph of the sensor interface in 40 nm CMOS. 290

Fig. 8.28 Measured output spectrum of the sensor interface for a 1 V supply voltage and a 100 mV differential signal. The SNDR determines the effective number of bits since it takes the noise as well as the distortion into account. The maximum FoM is reached for a 700 kHz bandwidth 291

Fig. 9.1 Block diagram of the wireless RFID tag. The power supply and clock input of different building blocks are controlled by the digital control logic. The state diagram of the finite state

machine (*FSM*) is shown *at the top*. The length and content of the different states can be programmed by means of the shift register 296

Fig. 9.2 Overview of the digital logic on the WSN tag. The FSM relies on different counters to make the right state transitions. The transmitted data, including the preamble, are scrambled using an LFSR before they are sent to the UWB transmitter. The shift register is used to control the length of the different states, the data and the LFSR scrambling code 297

Fig. 9.3 Profile of the energy consumption during one burst. In the initial phase, only the clock circuit and the receiver are switched on. When a correct tag-ID is received, the digital logic and the transmitter are switched on. Next the preamble, data and finally also the sensor data are subsequently transmitted. Afterwards, the tag is switched off. 297

Fig. 9.4 Block diagram of the pulse generator and output stage with antenna. The capacitor *C* is used to set the correct pulse width 298

Fig. 9.5 Output waveform (*left*) and spectrum (*right*) of the UWB transmitter with a 250 Ω load resistor. When using an appropriate antenna, the output spectrum is filtered and fits nicely within the FCC mask (*dashed line*). The design of the antenna is discussed in [209] 299

Fig. 9.6 Received slow pulse train over a 50 cm wireless link. At higher distances, the received pulses disappear under the noise floor 300

Fig. 9.7 The digital logic mainly consists of counters and shift registers. All of them are built using this basic flipflop 301

Fig. 9.8 Block diagram of an *n*-bit programmable counter. The counter is set to the values in the shift register at the moment when PRG is set. 301

Fig. 9.9 Block diagram of 6-bit LFSR. The initial values as well as the used polynomial can be programmed through the shift register. Code lengths ranging from 1 to 63 bits can be generated using this hardware. 301

Fig. 9.10 Photograph of the automated multi-purpose measurement setup. The pcb *on the right* is a general-purpose PIC-controller platform with several human interface devices and a serial link to a PC or other measuring hardware. The board *on the left* contains all chip-specific hardware, going from DACs, to analog and digital buffers and digital potentiometers to steer the sensor interface. Both boards contain a controller, connected through an I²C link. The data shown on

the display is steered by the *left controller board* to easily detect any communication errors between both controllers 302

Fig. 9.11 Photograph of a bonded sample. **a** For the high-frequency signals mmcx connectors are used. **b** Photomicrograph of the wireless RFID tag 303

Fig. 9.12 The single-ended structure of the AM-detectors results in a high sensitivity to supply noise. Therefore, to improve the input sensitivity of the resulting tags, two connected dies have been used at measurement time. The supply coupling and sensitivity problem can be reduced by an improved detector topology, increased supply decoupling or the use of guard rings around the different blocks 304

Fig. 10.1 Graphical comparison between the proposed oscillator designs and the state of the art. **a** Shows the power consumption as a function of the available voltage range. Both parameters contribute to the possible burst length. **b** Shows the temperature sensitivity in combination with the supply voltage sensitivity. Important to note are the highly-accurate LC oscillators in the south-west corner, which have a high power consumption and need to be trimmed (the markers correspond to [3, 175, 177, 178, 234]). **c** Shows the noise as a function of the oscillator output frequency. It is clear that all implementations fall within the range of RC (IV-C) implementations 310

Fig. B.1 Typical block diagram of a harmonic (linear) oscillator (**a**). An oscillator with a linear feedback network and a nonlinear amplifier (**b**). 331

Fig. B.2 Output voltage waveform and injected current for different transconductance amplifiers with soft distortion. The non-linearity is necessary to control the amplitude but causes harmonics in the output waveform. The harmonics, on their turn, cause a small frequency drop.
a $Q = 10, i(v) = 1.5 \cdot v - 0.1 \cdot v^3$.
b $Q = 10, i(v) = 2.0 \cdot v - 0.1 \cdot v^3$ 335

Tables

Table 1.1	Summary of the target specifications	25
Table 2.1	Commonly used PSD functions to characterize the frequency stability of an oscillator signal	50
Table 3.1	Maximum limits of the phase noise FoM	89
Table 4.1	Comparison of some implementations from literature	134
Table 5.1	Overview of some key properties	158
Table 5.2	Comparison to the state of the art for the temperature-independent oscillator.	159
Table 5.3	Comparison to the state of the art for the voltage-independent oscillator.	171
Table 6.1	Overview of the measured key properties (12 samples)	203
Table 6.2	Comparison of the oscillator to the state of the art	206
Table 7.1	Overview of the key measurement properties (8 samples)	236
Table 7.2	Overview of the implemented prototype versions	237
Table 7.3	Overview of the key measurement and simulation properties (5 samples)	251
Table 7.4	Comparison of the injection-locked clock generators to the state of the art	255
Table 7.5	Comparison of the receiver to the state of the art	256
Table 8.1	The most important design parameters of the PWM-based sensor interface in 130 nm CMOS	279
Table 8.2	The most important design parameters of the PWM-based sensor interface in 40 nm CMOS	283
Table 8.3	Comparison of the key simulated properties of the two designs	288
Table 8.4	Overview of the key properties (5 samples)	289
Table 8.5	Comparison to the state of the art in sensor interfaces	291
Table 9.1	Comparison of the developed tag to the state of the art	305
Table 10.1	Comparison of the presented time references	309
Table B.1	Coefficients of the different harmonics of the output waveform for the example oscillator.	336

Table C.1	The Allan variance for different slopes of the PSD	346
Table C.2	Values of the different structure functions, corresponding to the different areas in the power-law noise spectrum.	348
Table C.3	τ -dependency of structure functions of deterministic and stochastic processes.	349
Table D.1	Comparison to the state of the art	351
Table D.2	Comparison to the state of the art: noise	353
Table D.3	Comparison to the state of the art: voltage dependency	354
Table D.4	Comparison to the state of the art: temperature dependency	356