Yield-Aware Analog IC Design and Optimization in Nanometer-scale Technologies

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Preface

Developments over the last decades in very large-scale integration technologies allowed meeting the increasing demand for faster, cheaper, and reliable electronic devices. One of the key factors to support those developments is the implementation of most high-level functions of the chip in digital circuitry, whose design is highly automated due to the adoption of mature electronic design automation (EDA) tools. While digital integrated circuits (ICs) design is mostly automated, its analog counterpart is supported by a set of independent tools, dedicated to each step of the design flow, and highly dependent on human intervention. The increasing demand in circuit performances and complexity of device models due to the aggressive IC technology down-scaling have led to the acceptance of new simulation-based optimization tools for analog IC sizing, thus increasing analog IC design flow efficiency. Most of those tools consider only nominal circuit parameters values during the optimization process. As devices shrink down into nanometer scale, the effects of process variation have become very important and not considering those effects during the optimization and sizing process may result in circuit solutions push to limits of performances and dangerously close to the boundary of feasibility. Therefore, including a prediction of the percentage of circuits that comply with circuit specifications after fabrication, i.e., the circuit parametric yield, in the sizing and optimization process is an important step to avoid expensive redesign iterations. Monte Carlo (MC) analysis is the most general and reliable technique for yield estimation, yet the considerable amount of time it requires has discouraged its adoption in population-based analog IC circuit sizing and optimization tools.

The new yield estimation methodology developed and presented in this book is able to reduce the time impact caused by MC simulations in the context of analog ICs yield estimation, enabling its adoption in optimization processes with population-based algorithms, such as genetic algorithm (GA), considering the yield as one of the optimization problem objectives. The proposed methodology reduces the total number of MC simulations required to evaluate the optimization algorithm population. The reduction in the total number of simulations is achieved

because at each GA generation the population is clustered and only the representative individual from each cluster is subject to MC simulations. Initial tests using a modified version of the k-means clustering algorithm, to identify similar individuals in the GA population, and a new technique to select the cluster representative individuals were able to achieve a reduction rate up to 91% in the total number of MC simulations, when compared to the number of MC simulations required to evaluate the complete GA population.

The need to balance the trade-off between yield estimation accuracy and the reduction rate of MC simulations made the k-means methodology to evolve and search for different clustering techniques. A new version of the developed yield estimation methodology with reduced time impact from MC simulations was finally developed and implemented in a state-of-the-art analog IC sizing tool using the fuzzy c-means clustering algorithm. The new methodology based on fuzzy c-means and named FUZYE is able to achieve good yield estimation accuracy and high reduction rates in MC simulations. The FUZYE methodology shows that the yield for the rest of the nonsimulated individuals in the population can be accurately estimated based on the membership degree of fuzzy c-means and the cluster representative individuals yield values alone. This new method was applied on several circuit sizing and optimization problems, and the obtained results were compared to the exhaustive approach, where all individuals of the population are subject to MC analysis. The FUZYE methodology presents on average a reduction of 89% in the total number of MC simulations, when compared to the exhaustive MC analysis over the full population. Moreover, other important clustering algorithms were also tested and compared with the proposed FUZYE, with the latest showing an improvement up to 13% in yield estimation accuracy.

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Contents

Abbreviations

AC	Alternate current
ACO	Ant colony optimization
ADC	Analog-to-digital converter
ADE	Analog design environment
ADS	Advanced design system
AIDA	Analog integrated circuit design automation
AMG	Analog module generator
AWE	Asymptotic waveform evaluation
BMF	Bayesian model fusion
BV	Basic variables
CAGR	Compound annual growth rate
CMOS	Complementary metal-oxide-semiconductor
CW	Cloud width
DAC	Digital-to-analog converter
DC	Direct current
DE	Differential evolution
DOE	Design-of-experiments
EA	Evolutionary algorithms
EDA	Electronic design automation
FCM	Fuzzy C-means
FoM	Figure-of-merit
FUZYE	Fuzzy c-means based yield estimation
GA	Genetic algorithm
GBW	Gain-bandwidth product
GDC	Gain DC
GP	Geometric programming
GSA	Gravitational search algorithm
GUI	Graphical user interface
HAC	Hierarchical agglomerative clustering

HAD	Hierarchical analog design
HSMC	High-sigma Monte Carlo
IBS	Importance boundary sampling
IBY	Individual-based yield
IC	Integrated circuit
ICs	Integrated circuits
IRDS	International roadmap for devices and systems
IS	Importance sampling
ISE	Infeasible solution elimination
KMD	K-Medoids
KMS	K-Means
LAA	Linear assignment algorithm
LDS	Low discrepancy sequence
LHS	Latin hypercube sampling
LNA	Low noise amplifier
LP	Linear programming
MADS	Mesh adaptive direct search
MC	Monte Carlo
MCS	Monte Carlo pseudo-random sampling
MOEA/D	Multi-objective evolutionary algorithm based on decomposition
MOPSO	Multi-objective particle swarm optimization
MOSA	Multi-objective simulated annealing
MPI	Message passing interface
NBV	Non-basic variable
NMOS	n-Channel MOSFET
NSGA-II	Nondominated sorting genetic algorithm-II
OAD	Orthogonal array design
OCBA	Optimal computing budget allocation
OO	Ordinal optimization
OpAmp	Operational amplifier
OPDK	Organic process design kit
ORDE	Optimization-based random-scale differential evolution
OTA	Operational transconductance amplifier
OTFT	Organic thin-film transistors
PAD	Procedural analog design
PC	Partition coefficient
PCA	Principal component analysis
PDF	Probability density function
PDK	Process design kit
PDKs	Process design kits
PE	Partition entropy
PLL	Phase locked loop
PMOS	p-Channel MOSFET
POF	Pareto optimal front

PRSA	Parallel recombinative simulated annealing
PSA	Pattern search algorithm
PSO	Particle swarm optimization
PVT	Process voltage and temperature
QMC	Quasi-Monte Carlo
RF	Radio frequency
RSM	Response surface methodology
s.t.	Subject to
SA	Simulated annealing
SBX	Single binary crossover
SoC	System-on-chip
SPS	Stochastic pattern search
SQP	Sequential quadratic programming
SR	Sparse regression
SSS	Scaled sigma sampling
SVM	Support vector machine
UD	Uniform design
VLSI	Very large-scale integration
WCD	Worst-case distance
WCP	Worst-case performance
WCPF	Worst-case pareto front
XML	Extensible markup language

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