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Thomas Owen James

# A Hardware Track-Trigger for CMS

at the High Luminosity LHC

Doctoral Thesis accepted by  
Imperial College London, London, UK

 Springer

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*For Grandma, who inspired a curiosity  
and love for all things science and the natural  
world. I hope that this would have made  
you proud.*

# Supervisor's Foreword

The background to Tom James' thesis originates in the requirement to upgrade the CMS experiment at the CERN Large Hadron Collider to extend the studies of physics in the TeV energy range and continue searches for new phenomena for another couple of decades. To make this possible, large parts of the original experiment must be replaced, since they have been exposed to extremely high particle fluxes and will have been damaged by irradiation. At the same time, to successfully study rare processes, including the properties of the Higgs boson first observed in 2012, it will be necessary to acquire even larger event samples and increase the statistical sensitivity of the experiment. This will be made possible by increasing the area and granularity of some of the detectors, especially those closest to the colliding beams, which measure the trajectories of the particles emerging from the collisions. However, even with the fastest and most sensitive electronics available today, it is impossible to capture and store all the data from CMS so it is essential to select events of potential interest using a 'trigger', in which certain characteristics, such as the presence of a very high transverse momentum lepton, signal the possibility of an event of more than usual interest. The electronic trigger for CMS has evolved considerably from its original conception, but still mainly relies on signals from the muon detectors and electromagnetic and Hadron calorimeters. In the future, these signals alone are insufficiently selective to reduce the trigger rate to levels with which CMS can cope. The only way which has been found to improve on this is to exploit information from the tracking detectors in the experiment, which has hitherto not been used. This is immensely challenging, because the number of tracking elements is huge; for triggering purposes, about 13,000 modules comprising about 214 million sensor elements must be used. Studies have demonstrated that the tracking system must provide essentially all fully reconstructed trajectories for particles with transverse momentum above 2 GeV/c and these must be available for the trigger within a few microseconds. This is unprecedented, and especially difficult in a Hadron collider environment which generates multiple events per beam crossing with a very large number of outgoing charged particles from each interaction. Tom's thesis explains how this problem has essentially been solved, even though the final implementation of a system to

achieve it has yet to be built, and his, important, role in demonstrating how this will be done. It builds on work carried out, largely at Imperial College, to develop digital electronic hardware to process data from the CMS electromagnetic calorimeter for the Level-1 trigger. Over about twenty years, our group has developed a high level of expertise in programmable digital electronics, based on devices known as FPGAs, which has led to a series of processing boards, which are highly flexible and adaptable to many different problems. Most recently, new concepts were also proposed by our group to deliver a more powerful and flexible trigger for CMS using a time-multiplexing method, which offers many advantages for trigger systems. We decided to attack the track reconstruction problem by applying this new concept. Tom joined the effort in the final year of his undergraduate degree, working initially on software simulations of the tracking problem in CMS. When he started his Ph.D. work the following year, he was well prepared to tackle the full challenge of designing a system and demonstrating how track reconstruction could be implemented using current technology. The subject of Tom's Ph.D., therefore, evolved into a study of how a track-finder could work in CMS to provide the necessary reconstructed high transverse momentum tracks to the L1 trigger with high efficiency, within the available latency. We were able to build a demonstrator system to prove the concept would work by using existing FPGA boards, which had been designed originally for the calorimeter trigger. As the system design, and processing algorithms, evolved we were able to see how it could be made to work and build software and other processing infrastructure to test the idea and, importantly, to be able to compare the results from the FPGA processors with those from realistically simulated CMS events. During his Ph.D., Tom was based in CERN for about 18 months, with the task of implementing our track-finder demonstrator system, collaborating with a few other Imperial staff based there and in London. The success of the demonstrator considerably exceeded what most of us thought was likely initially, and owed much to Tom's efforts. He pushed himself very hard and was dedicated to it, working very long hours to solve any problem he encountered, invariably successfully. Tom demonstrated a remarkable flair for instrumentation work and gained much expertise in advanced software, electronic hardware and the rather complex tools and firmware required to operate modern programmable electronics based on FPGAs, as well as hands-on experience in computer and detector readout systems for real-time data acquisition. His thesis will be a reference for newcomers to the track-finder work for a long time to come. In his thesis, Tom acknowledges many others who contributed to this big task, but I would like to specially emphasise the important long-standing support we have received from our local funding agency, the UK Science and Technology Funding Council.

London, UK  
November 2019

Prof. Geoffrey Hall

# Abstract

The Compact Muon Solenoid (CMS) experiment at the Large Hadron Collider (LHC) is designed to study a wide range of high-energy physics phenomena. It employs a large all-silicon tracker within a 3.8 T magnetic solenoid, which allows precise measurements of transverse momentum ( $p_T$ ) and vertex position.

This tracking detector will be upgraded to coincide with the installation of the high-luminosity LHC, which will provide up to about  $10^{35}/\text{cm}^2/\text{s}$  to cms, or 200 collisions per 25 ns bunch crossing. This new tracker must maintain the nominal physics performance in this more challenging environment. Novel tracking modules that utilise closely spaced silicon sensors to discriminate on track  $p_T$  have been developed that would only allow the readout of hits compatible with  $p_T > 2\text{--}3$  GeV tracks to off-detector trigger electronics. This would allow the use of tracking information at the Level-1 trigger of the experiment, a requirement to keep the Level-1 triggering rate below the 750 kHz target, while maintaining physics sensitivity.

This thesis presents a concept for an all field-programmable gate array (FPGA)-based track-finder using a fully time-multiplexed architecture. A hardware demonstrator has been assembled to prove the feasibility and capability of such a system. The track-finding demonstrator uses a projective binning algorithm called a Hough transform to form track-candidates, which are then cleaned and fitted by a combinatorial Kalman filter. Both of these algorithms are implemented in FPGA firmware. This demonstrator system, composed of eight Master Processor Virtex-7 (MP7) processing boards, is able to successfully find tracks in one-eighth of the tracker solid angle at a time, within the expected 4  $\mu\text{s}$  latency constraint. The performance for a variety of physics scenarios is studied, as well as the proposed scaling of the demonstrator to the final system and new technologies.



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# Acronyms

ADC	Analog-to-digital converter
AIDA	Advanced European Infrastructures for Detectors at Accelerators
ALICE	A Large Ion Collider Experiment
AM	Associative Memory
AM06	Associative Memory 06
AMC	Advanced Mezzanine Card
AMC13	Advanced Mezzanine Card 13
ASIC	Application-specific integrated circuit
ATCA	Advanced Telecommunications Computing Architecture
ATLAS	A Toroidal LHC Apparatus
BDT	Boosted decision tree
BRAM	Block random access memory
BX	Bunch crossing
CBC	CMS binary chip
CERN	The European Organization for Nuclear Research
CIC	Concentrator integrated circuit
CMOS	Complementary metal-oxide semiconductor
CMS	Compact Muon Solenoid
CMSSW	CMS software
CPLD	Complex programmable logic device
CPU	Central processing unit
CSC	Cathode strip chambers
DAQ	Data Acquisition
DDR	Double data rate
DQM	Data quality monitoring
DR	Duplicate removal
DSP	Digital signal processor
DT	Drift tubes
DTC	Data, trigger and control
DTH	DAQ and Timing Hub

ECAL	Electromagnetic calorimeter
ES	Electromagnetic preshower
EU	European Union
FC7	FPGA Mezzanine Card Carrier Kintex-7
FF	Flip flop
FIFO	First in, first out
FILO	First in, last out
FNAL	Fermi National Accelerator Laboratory
FPGA	Field-programmable gate array
FTK	Fast TracKer
GBT	Gigabit transceiver
GLIB	Gigabit Link Interface Board
HB	HCAL barrel calorimeter
HCAL	Hadronic calorimeter
HDL	Hardware description language
HE	HCAL endcap calorimeter
HEP	High-energy physics
HF	HCAL forward calorimeter
HGCal	High-granularity calorimeter
HLHLS	High-level hardware description language
HL-LHC	High-luminosity Large Hadron Collider
HLS	High-level synthesis
HLT	High-level trigger
HT	Hough transform
HTP	Hough transform preprocessor
ILA	Integrated logic analyser
IP	Interaction point
IPbus	Internet protocol bus
IPMI	Intelligent Platform Management Interface
IT	Inner tracker
JTAG	Joint Test Action Group
KF	Kalman filter
KU-115	Xilinx Kintex Ultrascale 115
L1	Level-1
LHC	Large Hadron Collider
LHCb	Large Hadron Collider beauty experiment
LIFO	Last in, first out
LILO	Last in, last out
LpGBT	Low-power gigabit transceiver
LS3	Long Shutdown 3
LUT	Lookup tables
MaPSA	Macro-pixel sub-assembly
MCH	MicroTCA Carrier Hub
MGT	Multi gigabit transceiver
MicroGT	Micro Global Trigger

MicroHAL	Micro Hardware Access Library
microSD card	Micro Secure Digital Card
MicroTCA	Micro Telecommunications Computing Architecture
MP7	Master Processor Virtex-7
MP7-XE	Master Processor Virtex-7 Extended Edition
MPA	Macro-pixel ASIC
MTP	Multi-fibre Termination Push-on
NIM	Nuclear Instrumentation Module
OT	Outer tracker
PC	Personal computer
PCA	Principal component analysis
PCB	Printed circuit board
PCIe	Peripheral component interconnect express
PRM	Pattern Recognition Mezzanine
PS	Proton synchrotron
QCD	Quantum chromodynamics
QDR	Quad data rate
RAM	Random access memory
RCMS	Run control and monitoring system
RMS	Root mean square
RPC	Resistive plate chambers
RTM	Rear transition module
SATA	Serial advanced technology attachment
SERDES	Serialisation/De-serialisation
SEU	Single event upset
SFLR	Seed filter and simple linear regression
SM	Standard model of particle physics
SPS	Super proton synchrotron
SRAM	Static RAM
SSA	Strip sensor ASIC
TFP	Track-finding processor
TIF	Tracker integration facility
TLU	Trigger logic unit
USB	Universal Serial Bus
V7-690	Xilinx Virtex-7 XC7VX690T
VHDL	Very high speed integrated circuit HDL
VL+	Versatile Link PLUS
VU-11P	Xilinx Virtex Ultrascale 11+
VU-9P	Xilinx Virtex Ultrascale 9+
WLCG	Worldwide LHC computing grid
XDAQ	Cross-application Data Acquisition software