SOC (System-on-a-Chip) Testing for Plug and Play Test Automation

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Foreword

"As custom-configured chips carve out a larger portion of the microprocessor market, major changes are in store for the way chip fabrication facilities operate. To understand why, consider the underlying trends. One is the ever-increasing abundance of transistors on a chip, which portends a day when the number of chips per product will approach one..." This quotation from a recent article by Bass and Christensen (IEEE Spectrum, vol. 39, no. 4, p. 38. April 2002) describes just one of the changes in technology that lead us to the system-on-a-chip (SOC). They call the core-based SOCs as the "disruptive technology" and line up arguments showing that these are likely to dislodge today's high-performance microprocessor chips from their industry-favorite position.

This is the beginning of exciting times. Looking back over a period of fifty years we see printed-circuit boards going through phases of development from discrete components to discrete-chips and multi-chip modules. With each phase came new materials, design algorithms, performance criteria, heat dissipation problems, and manufacturing and test technologies. We can see the history repeating. To cite an example, we learned a great deal about signal propagation on the board interconnects, but must do still more to solve the problems of signal propagation on SOC interconnects. Of course, we can build upon the previous knowledge.

Interconnects may be just one problem. To test the SOCs we have to deal with new situations. Access to embedded cores, test data volume, at-speed test, fault diagnosis, power dissipation, test time, and test scheduling are some of the other problems for which solutions have already started emerging.

We have timed this special issue of JETTA for those readers who want to catch the new wave. The guest editor, Krishnendu Chakrabarty, issued an open call for papers about a year ago. We had an enthusiastic response from authors. He then selected the papers appearing here through the journal's peer review process. Unfortunately, not all the submitted papers could be accepted. A large variety of topics are covered in the articles appearing here and we believe this collection will have a lasting value. Therefore, this special issue is also being published as a book in the Frontiers in Electronic Testing series.

I am grateful to Krishnendu for meticulously handling all editorial responsibilities. My thanks to the authors and reviewers for their excellent contributions.

Vishwani D. Agrawal
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Preface

System-on-a-chip (SOC) integrated circuits composed of embedded cores are now commonplace. Nevertheless, there remain several roadblocks to rapid and efficient system integration. Test development is seen as a major bottleneck in SOC design, and test challenges are a major contributor to the widening gap between the design and manufacturing capabilities. Testing SOCs is especially challenging in the absence of standardized test structures, test automation tools, and test protocols. In addition, long interconnects, high density, and high-speed designs lead to new types of faults involving crosstalk and signal integrity.

This special issue of JETTA contains thirteen papers that address various aspects of SOC testing. These papers were selected after a thorough peer review process in which every paper received at least three reviews. The first paper by Marinissen et al. describes the proposed IEEE P1500 standard on embedded core testing. It provides an overview as well as technical details underlying the scalable wrapper architecture and the core test language envisaged in P1500. Papers 2–8 are on various aspects of test scheduling and test access mechanisms for core-based SOCs. Larsson and Peng describe an optimization framework for test scheduling, test access mechanism design, test set selection, and test resource placement. Huang et al. describe a power-constrained test scheduling approach based on two-dimensional bin-packing. In the third paper in this group, Koranne presents a reconfigurable wrapper design and a test scheduling algorithm for an SOC that employs reconfigurable wrappers. Marinissen shows how test protocols can be used for translating core-level tests to chip-level tests, and for test scheduling. In the next paper, Benabdenbi et al. describe a reconfigurable test access mechanism based on the use of a core access switch and test pattern compression/decompression. Basu et al. show how a test access mechanism switch can be used to test embedded cores and interconnect in an SOC. In the final paper of this group, Yoneda and Fujiwara show how transparent test data propagation in core-based SOCs can be achieved using the concept of consecutive testability.

Papers 9 and 10 propose solutions to the problem of high test data volume in SOCs. Jas and Touba describe how an embedded processor can be used for deterministic test vector compression and decompression. Next, Li et al. describe two schemes for compressing diagnostic test data for memory BIST. The last three papers are devoted to crosstalk, signal integrity, and faults affecting clock signals. Chen et al. describe a software-based self-test methodology that uses an embedded processor to detect interconnect crosstalk faults. Nourani and Attarha present fault models for signal integrity loss on interconnects in high-speed SOCs, and describe a BIST technique to detect noise and skew on the interconnects of such circuits. In the last paper, Metra et al. describe the design of an on-chip detector for on-line testing of faults affecting clock signals.

Finally, I take this opportunity to thank Editor-in-Chief Vishwani Agrawal for his strong support and encouragement for this special issue. I also thank all the authors for their timely submissions and the reviewers for their help.

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