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In July 1992, the International Symposium on Logic Synthesis and Microprocessor Architecture was held in Iizuka, Japan. The papers presented at the symposium were quite significant and we decided to publish the most outstanding of those concerned with Logic Synthesis and Optimization in textbook form for graduate students and young researchers.

There seem to be few textbooks of logic synthesis and optimization on the market. Thus, we would have no option but to turn to conference papers and journal papers to familiarize the students with the current status of research in the field, but we find most of them are just unsuitable for the students. Naturally, those papers are not education-oriented; they only offer a highly abstract description or explanation of the new ideas presented, mostly without any accompanying examples and illustrations, because of limited space.

To enhance their self-containedness, all the papers selected for publication here were reviewed by several people and were revised, in some cases extensively, and additional examples and illustrations, designed to increase the reader's understanding, were incorporated.

This book, which is organized into 16 chapters, deals with the following topics: Two-level minimization, Multi-level minimization, Application of binary decision diagrams, Delay optimization, Asynchronous circuits, Spectral method for logic design, Field programmable gate array design, EXOR logic synthesis, and Technology mapping.

I believe that the book covers the essential areas of logic synthesis and optimization and I hope that it will create a new interest and provide stimulation for organizing new courses at universities.
Overview of the Book

This book is divided into 16 chapters.

The first two chapters are concerned with the minimization of sum-of-products expressions. Rather than generating the set of all the prime implicants followed by the minimal covering of it, the first chapter shows a method to derive the set covering directly and implicitly from the given expression. The second chapter shows a new method to derive the set of prime implicants and essential prime implicants. These methods are useful for the functions with many variables that cannot be solved by the conventional methods.

The next four chapters, Chapters 3, 4, 5 and 6 discuss various design methods for multi-level logic networks. Chapter 3 introduces the basic concepts of the Transduction methods along with recent results. To design compact multi-level networks, we can use Network don’t cares and Boolean relation. Chapter 4 compares the effectiveness of these two approaches. For designing large networks, Chapter 5 presents a partitioning method while Chapter 6 presents partial collapsing method.

Binary Decision Diagrams (BDDs) are indispensable in logic synthesis. Chapter 7 shows a method to solve 0-1 integer programming problem by using BDDs.

In designing logic circuits, the speed is also important as well as the cost of the circuits. Chapter 8 considers delay models, while Chapter 9 reviews the asynchronous systems.

Logic design can be done more elegantly in the spectral domain rather than Boolean domain. Chapter 10 shows methods for functional decomposition, prime implicant generation and don’t care assignment by spectral methods.

It is predicted that in the future, most digital systems will be designed with microprocessors, memories and Field Programmable Logic Devices. Chapter 11 presents a design method for Field Programmable Gate Arrays (FPGAs) directly from BDDs.

The next three chapters discuss the EXOR logic synthesis. Chapter 12 introduces the minimization of exclusive-or sum-of-products expressions (ESOPs), and ESOP based logic synthesis, Chapter 13 reviews various classes of AND-EXOR expressions, and Chapter 14 shows a fast method to simplify ESOPs.
In many cases, multi-level logic networks are designed without considering the detail of the target electronic circuits, and then they are converted into the specific electronic logic circuits. This conversion is called technology mapping. The last two chapters are concerned with this process. Chapter 15 presents a method to perform factorization and technology mapping at the same time. Chapter 16 considers the sizing of the gates so that the total network delay meets the constraint while the total chip size is minimized.

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I also thank all the people who attended the Symposium, and the members of the Program Committee for the International Conference on Logic Synthesis and Microprocessor Architecture.

I acknowledge with gratitude the generous financial support from the Kyushu Institute of Technology and Japanese companies which enabled us to hold the Symposium.

Discussion with Prof. M. Perkowski was quite helpful in the planning of this book. My special thanks go to him.

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