

Low-Power Smart Imagers for Vision-Enabled Sensor Networks

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*“Any sufficiently advanced technology is
indistinguishable from magic”*

Arthur C. Clarke

Preface

The research group on ‘Vision Chips’ of the Institute of Microelectronics of Seville has an accredited experience of more than 12 years dedicated to the design of CMOS smart imagers and focal-plane array processors. By conveying some amount of processing and memory close to the photosensors, we have built computationally powerful and efficient chips to solve early vision tasks. The philosophy behind is to adapt the system to the nature of the sensory signal. At the architectural level, we are exploiting the parallelism that is inherent to low-level vision tasks, dealing with a large amount of simple raw data. At the circuit level, we are exploiting the device physics in order to efficiently implement the required functionalities. For this, we are taking advantage of the relatively relaxed requirements on accuracy found for an isolated image pixel. In other words, a big part of the information conveyed by the visual stimulus is redundant, therefore the conventional scheme in which every individual pixel value is converted to digital prior to any processing is inefficient. Our proposal is to send part of the computational load, that one corresponding to a regular and repetitive one, to the focal plane where, concurrently with sensing, it can be carried out by simpler and more efficient circuits. This also avoids realizing too many data transfers to and from the system memory.

Wireless sensor networks represent a scenario in which efficiency in the computation is enormously valuable. One of the reasons to implement vision algorithms right at the sensor node is to avoid a heavy network traffic that will naturally imply an extraordinary power consumption. Therefore, the implementation of vision at the sensor node must be done under a restricted power budget, otherwise it would not make sense. Then, if we are providing a power efficient implementation of the heaviest vision tasks together with higher level processing and wireless communications, we will be establishing the basis for an autonomous network of distributed smart cameras, capable of implementing co-operative and collaborative vision algorithms.

This book represents a contribution to the design of vision hardware for this type of autonomous embedded systems. On one hand, power consumption constitutes the major limitation when it comes to implement this kind of systems. On the other hand, processing of the visual stimulus demands a heavy computational load to be handled under strict timing requirements. In order to conjugate these two conflicting facts, we are proposing a bottom-up approach. Starting at the transistor level, we

are able to design a very simple processing element. Indeed, this processing element is nearly useless if isolated. However, when organized as an interconnected array, it becomes part of a massively parallel processing lattice capable of carrying out different tasks very fast in a very efficient way. Supported by this array, we move upwards in our approach and address the design of a vision chip intended to deliver simplified scene representations at ultra low energy cost. This chip is especially suitable to be integrated into a *mote*, the elementary autonomous embedded system of wireless sensor networks. The final step in our bottom-up approach is related to the application of vision-enabled *motest* to a specific case: early detection of forest fires. All in all, the contributions of this work can be summarized by the following points:

- An ad-hoc design of vision hardware based on massively parallel analog focal-plane processing is proposed as the means to reach very high power efficiency in vision-enabled WSN nodes.
- Different processing primitives are defined in order to achieve focal-plane image simplification. All of them are supported by time-controlled linear diffusion and reconfigurable image plane division, featuring a power-efficient VLSI implementation.
- Despite the nonidealities of MOS transistors working in the ohmic region, a MOS-based RC network is capable of performing linear diffusion with moderate accuracy. Furthermore, a design methodology for these networks has been developed in conjunction with an on-chip calibration process.
- A very compact circuitry capable of computing the image energy on a set of pixels is proposed.
- A QCIF-resolution vision chip prototype is reported. This chip, experimentally tested and fully functional, implements the processing primitives just mentioned above. Excellent results are achieved in terms of speed, area and power consumption, becoming a very competitive alternative when compared to similar chips found in the literature.
- This prototype has been integrated into a commercial WSN node, consuming only the 5.2% at most of the whole power consumption of the resulting vision-enabled wireless platform.
- A new framework based on vision-enabled WSNs is proposed to carry out early detection of forest fires. This framework presents better temporal and spatial resolution than current camera-based automatic systems.

The book is organized in seven chapters. In Chap. 1, the context for this work is introduced. A survey on vision-enabled WSN nodes is depicted in Chap. 2. Chapter 3 analyzes different primitives for image simplification based on focal-plane operators. Chapter 4 considers the VLSI implementation of linear diffusion and Chap. 5 reports the features of the vision chip that will be at the core of the system. Chapter 6 is dedicated to the description of a vision-enabled wireless node based on the already reported sensor chip. Finally, Chap. 7 deals with the details of a case study: early detection of forest fires.

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Abbreviations

ARM	Advanced RISC machine
CMOS	Complementary metal oxide semiconductor
CNN	Cellular nonlinear network
CPLD	Complex programmable logic device
DFT	Discrete Fourier transform
DNL	Differential non-linearity
ENOB	Effective number of bits
FFT	Fast Fourier transform
FOM	Figure of merit
FPGA	Field-Programmable Gate Array
GIS	Geographic information system
GPIO	General purpose input/output
INL	Integral non-linearity
LEO	Low earth orbit
LIDAR	Light detection and ranging
MAC	Multiple-accumulate operation
MCU	Microcontroller unit
MMC	Multimedia card
PAL	Phase alternating line
PCB	Printed circuit board
PDE	Partial differential equation
PE	Processing Element
PMIC	Power management integrated circuit
PWM	Pulse width modulator
QCIF	Quarter common intermediate format
RISC	Reduced instruction set computer
ROI	Region of interest
SAR	Successive approximation register
SIMD	Single instruction multiple data
SMA	Subminiature version A

SRAM	Static random access memory
UART	Universal asynchronous receiver-transmitter
UAV	Unmanned aerial vehicles
VGA	Video graphics array
VLSI	Very large scale integration
VCO	Voltage-controlled oscillator
WSN	Wireless sensor network

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