

**CMOS SINGLE CHIP FAST FREQUENCY
HOPPING SYNTHESIZERS FOR WIRELESS
MULTI-GIGAHERTZ APPLICATIONS**

ANALOG CIRCUITS AND SIGNAL PROCESSING SERIES

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CMOS Single Chip Fast Frequency Hopping Synthesizers for Wireless Multi-Gigahertz Applications

Design Methodology, Analysis, and Implementation

By

TAOUFIK BOURDI

Beceem Communications Inc., Santa Clara, California, USA

and

IZZET KALE

*Westminster University, London, UK and Eastern Mediterranean University,
Famagusta, North Cyprus*

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Preface

Frequency synthesizers are at the heart of the each transmitter/receiver system. Almost every communications consumer product employs a frequency synthesizer often operating as a local oscillator providing the carrier frequency of interest. Mobile phones, radios, and televisions are a few among the many applications that incorporate frequency synthesizers.

Recently, wireless local area network (WLAN) standards have emerged in the market. Those standards operate in various frequency ranges. To reduce component count, it is of importance to design a multimode frequency synthesizer that serves all WLAN standards including 802.11a, b, and g standards. With different specifications for those standards, designing integer-based phase-locked loop frequency synthesizers can not be achieved. Fractional-N frequency synthesizers offer the solution required for a common multimode local oscillator. Those fractional-N synthesizers are based on delta-sigma modulators which in combination with a divider yield the fractional division required for the desired frequency of interest.

In this book, the authors outline detailed design methodology for fast frequency hopping synthesizers for radio frequency (RF) and wireless communications applications. Great emphasis on fractional-N delta-sigma-based phase-locked loops from specifications, system analysis, and architecture planning to circuit design and silicon implementation.

The book describes an efficient design and characterization methodology that has been developed to study loop trade-offs in both open- and close-loop modeling techniques. This is based on a simulation platform that incorporates both behavioral models and measured/simulated subblocks of the chosen frequency synthesizer. The platform predicts accurately the phase noise, spurious and switching performance of the final design. Therefore,

excellent phase noise and spurious performance can be achieved while meeting all the specified requirements. The design methodology reduces the need for silicon re-spin enabling circuit designers to directly meet cost, performance, and schedule milestones.

The developed knowledge and techniques have been used in the successful design and implementation of two high-speed multimode fractional-N frequency synthesizers for the IEEE 801.11a/b/g standards. Both synthesizer designs are described in details.

NOMENCLATURE

abstol	Absolute Tolerance (Cadence™ specific)
AC	Alternating Current
ADC	Analog-to-digital converter
ASIC	Application-Specific Integrated Circuit
Balun	Balanced to unbalanced
BER	Bit Error Rate
CCK	Complementary CodeKeying
CLA	Carry Look-Ahead
CML	Current-Mode Logic
CP	Charge Pump
DAC	Digital-to-analog converter
dBc/Hz	Decibels per Hertz, SSB Phase Noise PSD Relative to the Carrier
DC	Direct Current
DCOC	DC Offset Cancellation
DFF	Data-type Flip-Flop
DGA	Digitally Controlled Variable-Gain Amplifier
Div	Divider
DMD	Dual-Modulus Divider
D-S	Delta–Sigma
DSC	Differential to Single-Ended Converter
DSSS	Direct-Sequence Spread Spectrum
EVM	Error Vector Magnitude
F	Noise Figure
FDC	Frequency to Digital Converter
FOM	Figure of Merit
IC	Initial Condition
IF	Intermediate Frequency
Inv	Inverter
IP	Intellectual Property
L(f)	Single-Sideband Phase Noise
LF	Loop Filter
LPF	Low-Pass Filter
LTI	Linear Time Invariant
LTV	Linear Time Variant
LUT	Lookup Table
MC	Modulus Control
MLF	Micro-Lead Frame

MMD	Multimodulus Divider
NTC	Negative Temperature Coefficient Capacitor
PA	Power Amplifier
PCB	Printed Circuit Board
PFD	Phase-Frequency Detector
PLL	Phase-Locked Loop
PRBS	Pseudorandom Binary Sequence
PSD	Power Spectral Density
PSDMD	Phase Switching Dual-Modulus Divider
PVT	Process Voltage Temperature
QAM	Quadrature-Amplitude Modulation
QPSK	Quadrature Phase-Shift Keying
Ref	Reference
Reltol	Relative Tolerance (Cadence™ specific)
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuit
Rx	Receiver
SS	Steady State
SSB	Single Sideband
SSBN	Single-Sideband Noise
SSBPSD	Single-Sideband Power Spectral Density
TCXO	Temperature-Compensated Crystal Oscillator
TDC	Time to Digital Converter
TFF	Toggle Flip-Flop
TRx	Transceiver
Tx	Transmitter
VCO	Voltage-Controlled Oscillator
VCXO	Voltage-Controlled Crystal Oscillator
VGA	Variable-Gain Amplifier
Vtune	VCO Tuning Voltage
WLAN	Wireless Local Area Network