Advanced Nanoscale ULSI Interconnects: Fundamentals and Applications

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Editors

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This book is dedicated to my wife Anat for all her support and patience.

Preface

In **Advanced ULSI interconnects – fundamentals and applications** we bring a comprehensive description of copper-based interconnect technology for ultra-large-scale integration (ULSI) technology for integrated circuit (IC) application. Integrated circuit technology is the base for all modern electronics systems. You can find electronics systems today everywhere: from toys and home appliances to airplanes and space shuttles. Electronics systems form the hardware that together with software are the bases of the modern information society. The rapid growth and vast exploitation of modern electronics system create a strong demand for new and improved electronic circuits as demonstrated by the amazing progress in the field of ULSI technology. This progress is well described by the famous "Moore's law" which states, in its most general form, that all the metrics that describe integrated circuit performance (e.g., speed, number of devices, chip area) improve exponentially as a function of time. For example, the number of components per chip doubles every 18 months and the critical dimension on a chip has shrunk by 50% every 2 years on average in the last 30 years. This rapid growth in integrated circuits technology results in highly complex integrated circuits with an increasing number of interconnects on chips and between the chip and its package. The complexity of the interconnect network on chips involves an increasing number of metal lines per interconnect level, more interconnect levels, and at the same time a reduction in the interconnect line critical dimensions.

The continuous shrinkage in metal line critical dimension forced the transition from aluminum-based interconnect technology, that was dominant from the early days of modern microelectronics, to copper-based metallization that became the dominant technology in recent years. As interconnect critical dimensions shrank to the nano-scale range (below 100 nm) more aggressive interconnect designs on smaller scale became possible, thus keeping "Moore's law" on pace. In addition to the introduction of copper as the main conducting material, it was clear that new dielectric materials, with low dielectric constant ("low-k" materials), should replace the conventional silicon dioxide interlevel dielectric (ILD). Thus the overall technology shift is from "aluminum–silicon dioxide" ULSI interconnect technology to "copper-low-k" technology. The Cu-low-k technology allows patterning of 45 nm wide interconnects in mass production and will probably allow further shrinkage in patterning of 15–22 nm lines in the next 10 years.

Copper metallization is achieved by electrochemical processing or processes that involve electrochemistry. The metal deposition is done by electrochemical deposition and its top surface is planarized (i.e., made flat or planar in the industry jargon) by chemical mechanical polishing (CMP). Electroplating is an ancient technique for metal deposition. Its application to ULSI technology with nano-scale patterning was a major challenge to scientists and engineers in the last 20 years. The success in the introduction of copper metallization so that it became the leading technology demonstrated the capability and compatibility of electrochemical processing in the nano-scale regime. In this book we will review the basic technologies that are used today for copper metallization for ULSI applications: deposition and planarization. We will describe the materials that are used, their properties, and the way they are all integrated. We will describe the copper integration processes and a mathematical model for the electrochemical processes in the nano-scale regime. We will present the way we characterize and measure the various conducting and insulating thin films that are used to build the copper interconnect multilayer structures using the "damascene" (embedded metallization) process. We will also present various novel nano-scale technologies that will link modern nano-scale electronics to future nano-scale-based systems.

Following this preface we bring an introduction where we bring the fundamentals of Cu electroplating for ULSI – when electrochemistry meets electrical engineering.

In Part II we give a historical review describing interconnect technology from the early days of modern microelectronics until today. It describes materials, technology, and process integration overview that brings into perspective the ways metallization is accomplished today. Further understanding of the scaling laws is presented next. Both semiconductor and interconnect progress are described, since they are interwoven into each other. Progress in interconnects always follows progress in transistor science and technologies. Although this book focuses on interconnect technology it should be clear that interconnects link transistors and the overall circuit operation is achieved by combined interaction of a highly complex network. The basic role of interconnects in such networks and how interconnects performance is linked to overall circuit performance are discussed next. One of the key issues in the increasing complex system is whether there are also other paradigms. One such paradigm is the 3D integration of ULSI components, also known as "3D integration."

In Part III we present a detailed review of interconnect materials. There is no doubt that the advancement in materials science and technology in recent years was the key to the advances in the ULSI technology. There are few groups of materials in ULSI interconnects: conductors (e.g., copper, silicides), barrier layers (e.g., Ta/TaN, TiN, WC), capping layers (dielectrics such as nitride-doped amorphous silicon or silicon nitride or electroless CoWP), and dielectrics with a dielectric constant less than that of silicon dioxide (i.e., low-k materials). We dedicate a special part to the material properties of silicides (metal–silicon compounds) that are used as the conducting interfacing material between the metallic interconnect network and the semiconductor transistors. The following parts bring an intensive review of low-k materials. They pose a major challenge since they should compete with

the conventional silicon dioxide that, although its dielectric constant is higher, has excellent electrical and mechanical properties and whose process technology is well established and entrenched in the industry and research communities.

In Part IV we focus on the actual electrochemical processes that are used for ULSI interconnect applications. We will first present the copper plating principles and their application to sub-micron patterning. Additives will be described in light of their role in the fully planar embedded metallization technology (i.e., the damascene process). In addition to conventional process we also mention some novel processes. Among them, the atomic layer deposition is the most promising and is under intensive investigation due to its ability to form ultra-thin seed layers with excellent uniformity and step coverage. Other interesting nano-scale processes are the deposition of nano particles, either inorganic or organic, that yield nano-scale metal lines that may, one day, be used for nano-electronics applications.

A common approach that links basic modeling to actual structure is the use of computer-aided design (CAD) simulating the desired structure based on the fundamental physical and chemical models of the process. For example, the use of electrochemical deposition onto narrow features with critical dimensions below 100 nm and with aspect ratio (i.e., the ratio of height to width) more than 2 to 1 requires a special process that is called "superfilling." In such a process, the filling of the bottom of the feature is much faster than the deposition on its upper "shoulders." Rapid deposition and full deposition onto the feature is achieved without defects (e.g., voids, seams) and with relatively thin metal on the shoulders that can be reliably removed in the ensuing chemical mechanical polishing planarization step. The discovery of the "superfilling" process was a major breakthrough in the initial stages of the introduction of copper metallization. In Part V we give a detailed description of such modeling of copper metallization using electrochemical processes for nano-scale metallization.

Part VI links all the previous parts together and describes the actual fully planar embedded metal process that is known as the damascene process. Following a detailed description of the various damascene concepts and its associated process steps we discuss the process integration issues. The integration involves linking all the various components: starting at the lithography level, patterning the wafer, deposition of the barrier and seed layers followed by the copper plating and its chemical mechanical polish (CMP) planarization, and ending with capping layer deposition. In this part we focus on the basic roles of each one of the components in the overall integration issue and on the way we put them all together.

Part VII describes the basic principles of the tools that are used for the copper metallization. There are two families of tools that we describe here – tools for deposition and tools for chemical mechanical polishing (CMP). Plating tools, both for electroplating and for electroless plating, are described in detail emphasizing their relation to the damascene process as applied for ULSI applications, i.e., material properties and integration in the manufacturing line.

Another family of tools is the one used for metrology and inspection. We present in Part VIII the innovative and advanced tools that are being used for Cu nanotechnology. One of the most promising tools is the use of X-ray technology, especially

X-ray reflection (XRR), which has proven to be the only method suitable for ultra-thin barrier layers and for porous materials that are used for low dielectric constant insulators. Another interesting development in modern planarization technology is the capability for in-line metrology. We present recent innovations in this field using optical metrology that is integrated with chemical mechanical polishing processes.

Finally, in Part IX we present a full and comprehensive review of the most promising interconnect technologies for future nanotechnology. This part includes a complete review of novel nanotechnologies such as bio-templating and nano-bio interfacing. Another key issue is the role of interconnect with future computation and storage technology. In this part we review the role of interconnect and 3D hyper integration, spintronics, and moletronics. In summary this part and the following prolog lay forth the reasons why electroplating is considered as the key technology for nano-circuits interconnects.

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