The g_m/I_D Methodology, A Sizing Tool for Low-voltage Analog CMOS Circuits

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The g_m/I_D Methodology, A Sizing Tool for Low-voltage Analog CMOS Circuits

The Semi-empirical and Compact Model Approaches

By

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Springer

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ISBN 978-0-387-47100-6 e-ISBN 978-0-387-47101-3
DOI 10.1007/978-0-387-47101-3
Springer Dordrecht Heidelberg London New York

Library of Congress Control Number: 2009940107

Printed on acid-free paper

Springer is part of Springer Science+Business Media (www.springer.com)

to Denise
and
to my parents
Oscar Jespers
and Mia Carpentier

Foreword

IC designers appraise currently transistors sizes while having to fulfill simultaneously a large number of objectives like a prescribed gain-bandwidth product, minimal power consumption, minimal area, low-voltage design, dynamic range, non-linear distortion, etc. Making appropriate decisions is not always obvious. How to meet gain-bandwidth specifications while minimizing power consumption of an Op. Amp without area penalty? Should moderate inversion be preferred to strong inversion? Is sizing an art or a mixture of design experience and repeated simulations? Or is it a constrained multivariate optimization problem? Optimization algorithms are attractive without doubt but they require translating not always well-defined concepts into mathematical expressions. The interactions amid semiconductor physics and systems are not always easy to implement.

The objective of the book is to devise a methodology enabling to fix currents and transistors widths of CMOS analog circuits so as to meet specifications such as gain-bandwidth while optimizing attributes like low power and small area. A special attention is given to low-voltage circuits. The sizing method takes advantage of the g_m/I_D ratio and makes use of either 'semi-empirical' data or compact models. The 'semi-empirical' approach utilizes large look-up tables derived from physical measurements carried out on real transistors or advanced models. The compact model approach offers the possibility to make use of analytic expressions. Unfortunately when it comes to real transistors, especially sub-micron devices, this isn't true anymore. Other means are necessary to keep track of high order effects without the risk to loose the inherent simplicity of compact models. Bias dependent instead of constant parameters offer the possibility to extend the validity of a model like the E.K.V. model.

In the first chapter, the Intrinsic Gain Stage, is sized making use of the classical strong and weak inversion large signal models of MOS transistors. This leaves open the moderate inversion region, a region that offers the best compromises generally as far as power consumption and sizes. To be able to size circuits in moderate inversion, we need a reliable large signal MOS model. The Charge Sheet Model that is considered in Chapter 2 is an invaluable tool for understanding the mechanisms governing current in MOS transistors, but it is not fitted for real transistors for it relies on the gradual channel approximation and makes use of mathematical expressions that are too complicated. The MATLAB tools that are available under

'extras.springer.com' overcome the mathematical aspects and offer the possibility to perform 'ideal experiments'. Some of the abstract aspects of the Charge Sheet Model moreover are bridged in Chapter 3 by the introduction of a graphical representation of the drain current that combines physical aspects and practical circuits.

The E.K.V. basic model discussed in Chapter 4, offers clearly more flexibility. It is an approximation of the Charge Sheet Model and a forerunner of what is viewed nowadays as compact Surface Potential Models. The model paves the way towards analytical expressions not only for the drain current but also for the terminal voltages whatsoever the mode of operation of the transistor, whether saturated or not. Unfortunately, the simple E.K.V. model is a gradual channel model like the Charge Sheet Model, unfit thus for real transistors, in particular short channel device.

The fact that drain currents predicted by the E.K.V. compact model look so similar to real drain currents opens the question whether the model could not be extended to real devices. In Chapter 5, we show that currents very close to real drain currents can be predicted when the parameters of the E.K.V. model vary with bias, even with 100 nm devices. The explanation may be the quasi-one-dimensional nature of the channel opposed to the two-dimensional space charge below the inversion layer. As a result, gradual channel conditions prevail in the inversion layer any longer than in the space charge when the gate length is shrinking. An algorithm is proposed to acquire the model parameters.

The Intrinsic Gain Stage is reconsidered in Chapter 6 in the light of the variable parameters compact model. Currents and transistor width obtained by means of the compact model reproduce very closely the values obtained by means of the 'semi-empirical' method. A series of examples considering a low-frequency and a one GHz gain-bandwidth product I.G.S. are described.

The remaining Chapters 7 and 8 extend the method respectively to the common-gate stage and to the basic Miller Op. Amp. The latter illustrates how to meet both, specifications and attributes. Specifications concern the gain-bandwidth product and phase margin, attributes low power and area. These determine optimal regions in the 2D sizing space defined by the first and second stages of the Miller Op. Amp. A MATLAB file compares design strategies.

I want to express my gratitude to Piet Wambacq for the opportunity he gave me to check the validity of the variable parameter E.K.V. model on a 90 nm technology developed by IMEC. I am also very thankful Prof. Gilbert Declerck, former President CEO and Ludo Deferm, executive vice-president of IMEC, who gave me permission to publish the results and the data listed under the 'extras.springer.com'.

My sincere thanks go to Prof. Fernando Silveira who published in 1996 the first paper illustrating the potential of the g_m/I_D methodology. I want to thank him as well as Prof. A. Vladimirescu for the very detailed comments and suggestions they made of the first chapters. I also want to associate Prof. D. Flandre to my thanks owing to our long-term collaboration at the Microelectronics lab of the Université Catholique de Louvain.

Though the specific current put to use in the book is the one defined in the E.K.V. model, I owe much to two research groups. I am indebted to Prof. Eric Vittoz for the

E.K.V. model, and to Prof. Carlos Galup-Montoro and Marcio C. Schneider for the A.C.M. model. I thank the supporters of the two models for motivating discussions and in particular the opportunity Prof. Montoro and Schneider gave me to visit them at the Federal University of Santa Catarina, Brasil.

Tervuren, July 2009 *P. Jespers*

Contents

Notations

A,A_{DC}, A_{AC}	voltage gain, DC and AC voltage gain
A.C.M.	Advanced Compact Model
C.L.M.	Channel Length Modulation
C.S.M.	Charge Sheet Model
C	capacitor value
C'_{ox}	gate oxide capacitance per unit area
C_{GB}	gate-to-substrate capacitance
C_{GD}	gate-to-drain capacitance
C_{GS}	gate-to-source capacitance
C_J	junction capacitance
C_{Jsw}	peripheral side-wall junction capacitance
C_{Jswg}	gate side–wall junction capacitance
C_m	Miller capacitance
CMOS	Complementary MOS
D	diffusion constant
D.I.B.L.	Drain Induced Barrier Lowering
E.K.V.	Enz, Krumenacher and Vittoz compact model
G.V.O.	Gate Voltage Overdrive voltage
g_d	output conductance
g_m	gate transconductance
g_{mb}	bulk transconductance
g_{ms}	source transconductance
i, i_F, i_R	normalized drain current, forward and reverse i
I.G.S.	Intrinsic Gain Stage
I_D	DC drain current
I_{Du}	unary DC drain current (W = L)
I_S	specific current
I_{Su}	unary specific current (W = L)
I_{Suo}	weak inversion unary specific current
L	gate length
N	impurity concentration
n	slope factor

PolyN,PolyP	mobility degradation polyn. of N- and P-channel transistors
q, q_F, q_R	normalized mobile charge density, forward and reverse q
qs, q_D	normalized mobile charge density at the source and drain
Q'_B	bulk charge density
Q'_i,	mobile charge density
Q'_t,	total charge density
R.H.P.	Right Half Plane zero
S_{VTo}	threshold voltage sensitivity factor with respect to V_{DS}
ThN,ThP	mobility degradation function of N- and P-channel transistors
U_T	thermal voltage *kT/q*
V, I, v, i	large and small signal voltage or current
V_A	*Early voltage*
V_S, V_G, V_D	source, gate and drain voltage with respect to substrate
V_{GS}, V_{DS}	gate and drain voltage with respect to the source
V_P, V_{PS}	pinch-off voltage with respect to the substrate or the source
v_{sat}	saturation velocity of mobile carriers
V_T	threshold voltage with respect to the substrate
V_{To}	threshold voltage with respect to the source
W	gate width
W.I, M.I, S.I	weak, moderate and strong inversion
β	μC'$_{ox}$ *W/L of MOS transistor*
γ	gamma of SPICE program
μ	mobility
μ_o	low-field mobility
ψ_S	surface potential
ω	angular frequency ($2\pi f$)
ω_c	angular cut-off frequency ($2\pi f_c$)
ω_{T}	angular transition frequency ($2\pi \mathrm{f}_T$)