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FAULT-TOLERANCE TECHNIQUES FOR
SRAM-BASED FPGAS

by

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Springer
Dedication

To my husband Christopher and to my parents Luiz Fernando and Ana Maria, who always gave me the support to follow my dreams.

“Fernanda Lima Kastensmidt”

To the future so that it can be appreciated by Erika while it arrives
To my parents, Cesare and Esther that have educated me on thinking about it.

“Luigi Carro”

To my wife Lucia, to my daughter Mariana, to my sons Guilherme and Eduardo, and to my parents Constantino and Maria de Lourdes.

“Ricardo Reis”
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Preface

This book presents fault-tolerant techniques for programmable architectures, the well-known Field Programmable Gate Arrays (FPGAs), customizable by SRAM. FPGAs are becoming more valuable for space applications because of their high density, high performance, reduced development cost and re-programmability. In particular, SRAM-based FPGAs are very valuable for remote missions because of the possibility of being reprogrammed by the user as many times as necessary in a very short period. SRAM-based FPGA and micro-controllers represent a wide range of components in space applications, and will be the focus of this work, more specifically the Virtex® family from Xilinx and the architecture of the 8051 micro-controller from Intel.

The content addressed in this book ranges from the study of state-of-the-art of SEU mitigation techniques for ASIC and FPGA components, to the implementation and test of new fault-tolerant techniques for SRAM-based FPGA components. In the first phase of the research presented in this text, available techniques to protect integrated circuits against radiation are studied. The radiation fault-tolerant techniques can be classified as: the ones that change the technology used in the fabrication process such as Silicon on Insulator (SOI), and the ones that change the hardware design of a system such as SEU hardened memory cells, error detection and correction codes (EDAC) and logic redundancy. There is a trade-off with each mitigation technique for each type of architecture system, and there is no best unique solution so far. Some of the considered techniques are evaluated in terms of area, cost and performance. The first case study circuit is the 8051 micro-controller from Intel (Intel, 1994). The microprocessor architecture was chosen for its representation of the majority of system requirements in space.
applications nowadays, presenting all types of logic to be protected and being part of the new generation architectures based on FPGA with an embedded hard microprocessor core.

The description of the 8051 micro-controller used in the experiment was developed at Federal University of Rio Grande do Sul (Carro; Pereira; Suzim, 1996). It is composed of a datapath unit, control unit, state machine, instruction decoding unit and embedded memory. Although the 8051 micro-controller has a simplified architecture compared to the latest available microprocessors, the assumptions made in its architecture can be adapted to any other processor-like circuit. Techniques such as hamming code and radiation tolerant flip-flops were implemented in the 8051 micro-controller (LIMA et al., 2000a; LIMA et al., 2000b). Fault injection (LIMA et al., 2001a; LIMA et al., 2002a; LIMA et al., 2002b) and simulation are used to analyze the efficiency of the techniques. Area and performance are taken into consideration with the results.

The second phase of the work presented in this book resumes the analysis of an SRAM-based FPGA and the SEU effects in this architecture. The Virtex® FPGA family from Xilinx is the most popular high density and high performance FPGA used in the market nowadays, and it was chosen to be the object of study in this work. There are two ways to mitigate SEU in FPGA designs, as previously mentioned. One is based in changing the FPGA architecture and the other one is based on modifying the high-level design description before the FPGA synthesis. First, implementations of some SEU mitigation techniques in the architectural level of the FPGA matrix are proposed. The SRAM-based architecture is divided in main blocks classified by functionality (such as LUT), flip-flops, customization routing, embedded memory, PLL, etc. SEU mitigation techniques for many of the blocks are discussed. The objective is to show the trade-off of each technique in the Virtex® FPGA and the complexity of developing a new architecture with changes at the mask level. This investigation is based on the experience collected in first phase.

Because of the limitations in developing and testing a new fault-tolerant FPGA architecture such as cost and time-to-market, techniques at the high-level description must also be investigated. The Triple Modular Redundancy (TMR) with voters is a common technique to protect against SEU in ASICs and it can be also applied to protect FPGAs against SEU, as shown in (Carmichael, 2001). In this case, the mitigation can be applied to the high-level design description language and synthesized in the device without any changes in the mask process. The TMR technique is first tested in the Virtex® architecture by using a small design based on counters. Faults are injected in all sensitive parts of the FPGA and a detailed analysis of the
effect of a fault in a TMR design synthesized in the Virtex® platform is performed.

In order to test a more complex design protected by TMR in the Virtex® platform that would also include embedded memories, the same 8051 like micro-controller description was protected by TMR and tested under the FPGA platform. There are many advantages of using the same design as the 8051 micro-controller, such as good description knowledge, importance of micro-controllers IP in FPGA and the possibility of comparison with the previous techniques (hamming code and SEU hardened memory cells) applied in the same description. The TMR 8051 micro-controller was tested by fault injection and under proton radiation in a ground facility (Lima et al., 2001b). At the end of these practical experiments (Lima et al., 2001b; Carmichael; Fuller; Fabula; Lima, 2001), the use of TMR in Virtex® FPGAs has confirmed the efficacy of the TMR structure to recover upsets in the FPGA architecture. However, the TMR technique presents some limitations, such as area overhead, three times more input and output pins and, consequently, a significant increase in power dissipation and also some robustness issues. The result has brought the necessity of improving this technique in order to reduce the overheads and to try to improve robustness as well.

In the third phase of the work, additional SEU mitigation techniques for the Virtex® FPGA architecture are investigated. A new high-level fault-tolerant technique for SRAM-based FPGA was developed (Lima, Carro, Reis, 2003a; Lima, Carro, Reis, 2003b). This technique combines time and hardware redundancy with some extra features able to cope with the effects of SEU in FPGAs, and at the same time it is able to reduce the number of input and output pads and area overhead compared to the traditional TMR approach. The methodology was validated in combinational and sequential circuits by using fault injection experiments emulated in a prototype board. Results have confirmed that this new technique can reduce not only pin count but also area as well, without compromising performance and reliability.

This book is organized as follows. Chapter 2 describes the radiation effects on integrated circuits manufactured using CMOS process and it explains in detail the difference between the effects of a SEU in ASIC and in SRAM-based FPGA architectures. This chapter shows the architecture analysis of the Virtex® FPGA and all its radiation sensitive area. Chapter 3 presents the main techniques, either being commercialized by companies or being studied by researchers, to mitigate the effects of radiation in ASICs, such as microprocessors and memories, and in programmable architectures, such as FPGAs programmed by SRAM and by antifuse technology.
Chapter 4 discusses some SEU mitigation techniques that can be applied at the FPGA architectural level. The FPGA is divided by functionality in main logic blocks. Each block has different characteristics, and the fault-tolerant technique must take into account the peculiarities of each. In the end, a SEU tolerant FPGA is proposed based on the presented SEU mitigation techniques.

Chapter 5 defines the problem of protecting SRAM-based FPGAs against radiation in the high level description. The Triple Modular Redundancy (TMR) technique in the high level description for FPGAs is addressed in this chapter. Chapter 6 evaluates the robustness of the TMR technique by using fault injection in the bitstream of the FPGA and also in a radiation ground test facility. In this chapter, a methodology is presented to relate the upset bit in the bitstream to the SRAM cell location in the user’s design floor-planning. The obtained results represent an important base for this work, because it shows the limitations of the TMR method on the SRAM-based FPGA, justifying the research of new design techniques for SEU mitigation in SRAM based FPGAs.

Chapter 7 shows the implementation and results of the 8051 description protected by TMR in the Virtex® FPGA. All implementation details of the TMR technique were carefully applied to the VHDL description of the 8051 to test this technique in a more complex design. The final protected design was tested by fault injection in the FPGA bitstream and also in a radiation ground test facility. Results and final remarks are placed at the end of that chapter.

Chapter 8 introduces a new high-level technique for designing fault tolerant systems for SRAM-based FPGAs, without modifications in the FPGA architecture, able to cope with transient faults in the user combinational and sequential logic, while also reducing pin count, area and power dissipation compared to the traditional TMR. The methodology is validated by fault injection experiments in VHDL description emulated in a prototyped board. Results in terms of fault coverage and area and performance comparison with the TMR approach are presented.

The technique presented in chapter 8 presents some limitations in fault coverage because it uses the standard time redundancy approach to detect the effect of a SEU in the FPGA matrix. In chapter 9, an improvement to the high-level technique presented in chapter 8 is proposed. This technique combines duplication with comparison and concurrent error detection technique in order to cope with the permanent effects of a SEU in FPGAs and at the same time to reduce TMR overheads. In addition, this proposed method is also able to detect physical faults, which are permanent faults that are not corrected by reconfiguration. The methodology is also validated by
fault injection experiments in an emulation board. Some fault coverage results and a comparison with the TMR approach are evaluated.

Final remarks are placed in chapter 10 followed by the references. Because the technology is constantly in evolution, there are always improvements to be made in the protection of integrated circuits, and consequently, in the way designs are protected against faults. This work has contributed to some solutions for the SRAM-based FPGAs that are being projected to work in commercial applications but are manufactured by nanotechnologies and need to work properly in the presence of upsets. However, there is much more research to be done as each step of investigation brings more questions and possibilities of solutions. As a result, future techniques are discussed in the final chapter of this book.