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DESIGN OF VERY HIGH-FREQUENCY MULTIRATE SWITCHED-CAPACITOR CIRCUITS
Extending the Boundaries of CMOS Analog Front-End Filtering

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Dedication

This book is dedicated to

Our Wives
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Preface

Integration of high-frequency analog filtering into the system Analog Front-End (AFE) is increasingly demanded for the ever growing high-speed communications and signal processing solutions with the corresponding advances in Integrated Circuit (IC) technology. Although the AFEs represent a small portion of the total mixed-signal system chip, they usually are its speed and performance bottleneck. Especially, the design of the AFEs becomes more and more challenging due to the continuous lowering of the supply and increasing of the operation speed, as well as noisying of the working environment driven by the constant growing digital signal processing (DSP) core.

This book presents a multirate sampled-data interpolation technique and its Switched-Capacitor (SC) implementation for very high frequency filtering (over hundreds of MHz) while having also dual inherent advantages of reducing the speed of the digital-to-analog converter and the DSP core together with the simplification of the post continuous-time smoothing filter.

The book is organized in eight chapters. This chapter presents an overview of the introductory aspects of the current state-of-the-art high-frequency SC filters and multirate filtering with emphasis on the SDA interpolation techniques for explicating the motivation and the objectives of the research work in this book.

Chapter 2 will describe the mathematical characterization of the conventional sampled-data analog interpolation with its input lower-rate S/H shaping distortion and will also introduce the ideal improved analog interpolation model with its traditional bi-phase SC structure implementation. Then, the development of the efficient multirate polyphase-based SC structures suitable for high-performance optimum-class improved analog
interpolation filtering will be proposed. Different low-sensitivity circuit topologies with both Finite Impulse Response (FIR) and Infinite Impulse Response (IIR) characteristics will be developed, respectively, for low and high selectivity filtering.

Chapter 3 will present the practical IC technology imperfections related to IC implementation of SC multirate circuits that will be comprehensively investigated with respect to the power requirement issue, capacitance ratio mismatches, finite gain and bandwidth, input-referred DC offset sensitivity effects of the opamps, timing random-jitter and fixed periodic skew in the multirate clock phase generation as well as filter overall noise performance. All those practical design considerations are very useful in high-speed sampled-data analog integrated circuit design.

Chapter 4 will present advanced circuit techniques, i.e. gain- and offset-compensations, specialized for multirate SC filters and that are necessary to alleviate the imperfections of the analog integrated circuitry. Such techniques will be explored first for the basic building blocks: mismatch-free SC delay cells and SC accumulator, and later the impacts in the compensation of the overall system response will also be addressed and demonstrated through specific examples for both multirate FIR and IIR SC interpolating filters. Furthermore, the practical design trade-offs for utilization of such techniques will also be analyzed with respect to the accuracy versus speed and power.

Chapter 5 will set forth the design and implementation of a low-power SC baseband interpolating filter for NTSC/PAL digital video restitution system with CCIR-601 standards. The filter, which employs several novel optimized structures including coefficient-sharing, spread-reduction, semi-offset-compensation, mismatch-shaping, double-sampling and analog multirate/techniques, achieves a linear-phase lowpass response with 5.5-MHz bandwidth, 108 Msample/s output from 13.5 Msample/s video input. Both behavior-, transistor- and layout-extracted level simulations will be presented for illustrating the effectiveness of the circuit in 0.35 µm CMOS technology.

Chapter 6 will describe the design and implementation of a 2.5 V, 15-tap, 57 MHz SC FIR bandpass interpolating filter with 4-fold frequency up-translation for 22-24 MHz inputs at 80 MHz to 56-58 MHz outputs at 320MHz to be used in a Direct-Digital Frequency Synthesis (DDFS) system for wireless communication also in 0.35 µm CMOS. Special design considerations in both filter transfer function, circuit architectures, circuit building blocks as well as specific layout techniques for dealing with non-ideal properties in realization of the high-speed analog and digital clock
circuits will be presented comprehensively in terms of the speed relaxation, noise and mismatching reduction.

**Chapter 7** will then present the Printed-Circuit Board (PCB) design, experimental testing setup, as well as the measured results of the prototype interpolating filter chip built for the DDFS system described in Chapter 5. In addition to the measurement summary, a comparison among previously reported SC filters will also be offered.

**Chapter 8** will finally draw the relevant concluding remarks.

**Appendixes** will be also provided for detailed mathematic derivation and analysis of the timing-skew errors in parallel sampled-data systems with S/H effects, namely, non-uniformly holding effects, and also the estimation scheme of the filter noise performance including opamp finite-gain and offset error analysis of SC building blocks.

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Rui Paulo Martins
José Epifânio da Franca
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List of Abbreviations

AAF : Anti-Aliasing Filter
AC : Alternating Current
ADB : Active Delayed-Block
ADC : Analog-to-Digital Converter
AFE : Analog Front-End
AIF : Anti-Imaging Filters
AZ : Autozeroing
BPF : Band-Pass Filter
C-DFII : Complete Direct-Form II
CAD : Computer-Aided Design
CDMA : Code Division Multiple Access
CDS : Correlated-Double Sampling
CM : Common Mode
CMOS : Complementary Metal Oxide Semiconductor
CMFB : Common-Mode Feedback
CMRR : Common-Mode Rejection Ratio
CQFP : Ceramic Quad Flat-Pack
CT : Continuous-Time
DAC : Digital-to-Analog Converter
DB : Differentiator-Based
DC : Direct Current
DDFS : Direct-Digital Frequency Synthesis
DF : Direct-Form
DFII : Direct-Form II
DR : Dynamic Range
DSP : Digital Signal Processing
DT : Discrete-Time
DUT : Device Under Test
DVD : Digital Video Disks
EC : Error-storage Capacitor
EM : Electromagnetic
EMC : Electromagnetic Compatibility
ENBW : Equivalent Noise Bandwidth
ER : Extra Ripple
FFT : Fast Fourier Transform
FIR : Finite-Impulse-Response
GBW : Gain BandWidth
GOC : Gain- and Offset-Compensation
H-CDS : Holding Correlated-Double Sampling
IC : Integrated Circuit
IF : Intermediate-Frequency
IIR : Infinite Impulse Response
IM3 : 3rd-order Intermodulation Distortion
IN-CON : Input & Output timing-correlatively, Nonuniformly sampled & played out
IN-OU : Input Nonuniformly sampled, Output Uniformly played out
IS : Impulse-Sampled
IU-ON : Input Uniformly sampled, Output Nonuniformly played out
I-V : Current-to-Voltage
LC : Inductive-Capacitive
LPF : Low-Pass Filter
LVS : Layout versus Schematic
MF : Mismatch-Free
MCP-DFII : Mixed Cascade/Parallel Direct Form II
MOS : Metal-Oxide Semiconductor
MUX : Multiplexer
NTSC : National Television Standards Committee
OFR : Open-floating Resistor
OIP3 : Output 3rd-order Intercept Point
OPAMP : operational amplifier
OTA : Operational Transconductance Amplifier
P-CDS : Predictive Correlated-Double Sampling
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<tr>
<td>P-DFII</td>
<td>Parallel Direct Form II</td>
</tr>
<tr>
<td>PAL</td>
<td>Phase Alternation Line</td>
</tr>
<tr>
<td>PC</td>
<td>Parallel-Cyclic</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed-Circuit Board</td>
</tr>
<tr>
<td>PCTSC</td>
<td>Parasitic-Compensated Toggle-Switched Capacitor</td>
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<tr>
<td>PM</td>
<td>Phase Margin</td>
</tr>
<tr>
<td>POG</td>
<td>Precise Opamp Gain</td>
</tr>
<tr>
<td>PSRR</td>
<td>Power Supply Rejection Ratio</td>
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<td>PSS-AC</td>
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<tr>
<td>QFP</td>
<td>Quad Flat-Pack</td>
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<tr>
<td>R-ADB</td>
<td>Recursive-ADB</td>
</tr>
<tr>
<td>RES</td>
<td>Rising-Edge Synchronizing</td>
</tr>
<tr>
<td>RF</td>
<td>Radio Frequency</td>
</tr>
<tr>
<td>ROM</td>
<td>Read-Only Memory</td>
</tr>
<tr>
<td>RUT</td>
<td>ROM Look-Up Table</td>
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<tr>
<td>SC</td>
<td>Switched-Capacitor</td>
</tr>
<tr>
<td>SDA</td>
<td>Sample-Data Analog</td>
</tr>
<tr>
<td>SDM</td>
<td>Sigma-Delta modulators</td>
</tr>
<tr>
<td>SDV</td>
<td>Switched Digital Video</td>
</tr>
<tr>
<td>SFDR</td>
<td>Spurious-Free Dynamic Range</td>
</tr>
<tr>
<td>S/H</td>
<td>Sample-and-Hold</td>
</tr>
<tr>
<td>SI</td>
<td>Switched-current</td>
</tr>
<tr>
<td>SMD</td>
<td>Surface-Mount Device</td>
</tr>
<tr>
<td>SINAD</td>
<td>Signal-to-Noise Plus Distortion Ratio</td>
</tr>
<tr>
<td>SNR</td>
<td>Signal-to-Noise Ratio</td>
</tr>
<tr>
<td>SSC</td>
<td>Same Sample Correction</td>
</tr>
<tr>
<td>T/H</td>
<td>Track-and-Hold</td>
</tr>
<tr>
<td>TDMA</td>
<td>Time Division Multiple Access</td>
</tr>
<tr>
<td>THD</td>
<td>Total Harmonic Distortion</td>
</tr>
<tr>
<td>TSC</td>
<td>Toggle-Switched Capacitor</td>
</tr>
<tr>
<td>TSI</td>
<td>Toggle-Switched Inverter</td>
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<tr>
<td>TV</td>
<td>Television</td>
</tr>
<tr>
<td>UC</td>
<td>UnCompensated</td>
</tr>
<tr>
<td>UGB</td>
<td>Unity-Gain Bandwidth</td>
</tr>
<tr>
<td>VCM</td>
<td>Common-Mode Voltage</td>
</tr>
<tr>
<td>VDSL</td>
<td>Video Digital Subscriber loop</td>
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