Compilation Techniques for Reconfigurable Architectures

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To Teresa, Rodrigo, and Frederico
(João M. P. Cardoso)

To Mariana de Sena and Rafael Nuno
(Pedro C. Diniz)

Preface

The extreme flexibility of reconfigurable architectures and their performance potential have made them a vehicle of choice in a wide range of computing domains, from rapid circuit prototyping to high-performance computing. The increasing availability of transistors on a die has allowed the emergence of reconfigurable architectures with a large number of computing resources and interconnection topologies. To exploit the potential of these reconfigurable architectures, programmers are forced to map their applications, typically written in high-level imperative programming languages, such as C or MATLAB, to hardware-oriented languages such as VHDL or Verilog. In this process, they must assume the role of hardware designers and software programmers and navigate a maze of program transformations, mapping, and synthesis steps to produce efficient reconfigurable computing implementations. The richness and sophistication of any of these application mapping steps make the mapping of computations to these architectures an increasingly daunting process. It is thus widely believed that automatic compilation from high-level programming languages is the key to the success of reconfigurable computing.

This book describes a wide range of code transformations and mapping techniques for programs described in high-level programming languages, most notably imperative languages, to reconfigurable architectures. While many of these transformations and mapping techniques have been developed in the context of compilation for traditional architectures and high-level synthesis, their application to reconfigurable architectures poses a whole new set of challenges, in particular when targeting fine-grained reconfigurable architectures such as contemporary Field-Programmable Gate-Arrays (FPGAs). Their ability to emulate virtually any execution paradigm and to configure their logic blocks as either storage or computing resources forces compilers to evaluate a huge number of possible mapping alternatives in search for effective hardware implementations on these reconfigurable architectures.

This book is primarily intended for researchers and graduate students in the areas of study of hardware compilation and advanced computing architectures in the fields of Electrical and Computer Engineering and Computer Science. As it focuses on the specific topic of compilation from high-level program descriptions to reconfigurable

architectures, this book can easily support advanced compiler and computer architecture courses related to reconfigurable computing. Through this book, we hope to motivate further discussions on the challenging topic of compilation for reconfigurable architectures, and also hope this book can be a reference for researchers, educators, and students to learn more about the most prominent efforts on this subject in recent years.

This book was only made possible with the unabated comprehension, relentless, and unconditional support of our families who allowed us to devote to it countless many hours, some of them late at night. It is to them we dedicate this book, in particular to Teresa, Rodrigo, Frederico, Mariana, and Rafael. We are also truly indebted to our parents, Cristina and Luís and Mariana and Mário, for their lifelong support and encouragement. Lastly, we would also like to thank our friends for their support and friendship.

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