DESIGN OF MULTI-BIT DELTA-SIGMA A/D CONVERTERS
Abstract

Over the last decade, a vast evolution of communication systems was observed. The enormous popularity and expansion of the internet was a driving force for the development of broadband internet access in every home to cope with the increasing bandwidth requirements for multimedia applications. At the same time, wireless communication evolved from an analog network with large devices, to small and cheap handsets which are based on digital communication standards. The core of all these complex electronic systems consists of digital circuits which have a huge computational power and are implemented in CMOS technologies. The development of ever faster and more powerful digital cores opens the way to more complex systems with increasing demands for the analog part which has to provide an interfacing layer to the outside world. One of the crucial building blocks in the analog part is the Analog to Digital converter.

The goal of this work is to present an architecture study of ΔΣ AD converters and to provide insight into a wide range of analog circuit imperfections which can limit the performance. The emphasis is put on high-speed high-resolution converters in CMOS, although the material can also be applied for other specification goals and technologies.

The first part of this work takes a closer look at various architectures of ΔΣ AD converters. These range from single-loop to cascaded and various multi-bit topologies. The operation and several stability issues of the converters are discussed. The various topologies are optimized to obtain stable converters with a high accuracy and a clear overview is provided of the maximum achievable performance of each topology. Finally, the linearity problem of the DA converter in the feedback loop of multi-bit converters is discussed, together with possible solutions.

The second part studies several design aspects of ΔΣ converters, with a special focus on multi-bit implementations. Various models are provided for a wide range of linear and non-linear circuit non-idealities which can degrade the performance of the converter. These models allow the designer to determine the required specifications for the different building blocks. A power estimation is presented and used to derive several design considerations.

The last part discusses the systematic design and measurement results of two implementations. The first is a cascaded 2-1-1 converter, implemented in a 3.3V 0.5μm standard CMOS technology. It achieves a dynamic range of 92dB for a Nyquist-rate of 2.2MHz. The second converter is a multi-bit third-order topology with Dynamic Element Matching to relax the linearity requirements for the DAC. It is implemented in a standard 0.65μm CMOS technology, achieves a dynamic range of 97dB and a Nyquist-rate of 2.5MHz.
List of Symbols and Abbreviations

Abbreviations

AD  Analog-to-Digital
ADC  Analog-to-Digital Converter
ADSL  Asymmetric Digital Subscriber Line
BiCMOS  Bipolar Complementary Metal Oxide Semiconductor
biDWA  Bi-Directional Data Weighted Averaging
C21  Cascaded Topology 2-1
C211  Cascaded Topology 2-1-1
C22  Cascaded Topology 2-2
CAD  Computer Aided Design
CLA  Clocked Averaging
CMOS  Complementary Metal Oxide Semiconductor
DA  Digital-to-Analog
DAC  Digital-to-Analog Converter
DC  Direct Current
DDS  Data Directed Scrambling
DEM  Dynamic Element Matching
DMT  Discrete Multi Tone
DR  Dynamic Range
$DR_i$  Input Dynamic Range
$DR_o$  Output Dynamic Range
DWA  Data Weighted Averaging
DWA O2  Second-Order Data Weighted Averaging
DWArand  Randomized Data Weighted Averaging
ENOB  Effective Number Of Bits
FDM  Frequency Division Multiplexing
FFT  Fast Fourier Transform
FM  Figure of Merit
FSM  Finite State Machine
HPF  High-Pass Filter
IC  Integrated Circuit
ILA  Individual Level Averaging
List of Symbols and Abbreviations

ISI  Inter Symbol Interference
LPF  Low-Pass Filter
LSB  Least Significant Bit
MSB  Most Significant Bit
MTPR Multi Tone Power Ratio
NMOS n-channel MOSFET
NRZ Non-Return-to-Zero code
OL  Overload level
OTA Operational Transconductance Amplifier
pdf Probability Density Function
PDWA Partitioned Data Weighted Averaging
PMOS p-channel MOSFET
POTS Plain Old Telephony System
PROM Programmable Read Only Memory
psd Power Spectral Density
QAM Quadrature Amplitude Modulation
RZ Return-to-Zero code
SDR Signal-to-Distortion Ratio
SFDR Spurious Free Dynamic Range
SNR Signal-to-Noise Ratio
SNR\textsubscript{p} Peak Signal-to-Noise Ratio
SNDR Signal-to-Noise-and-Distortion Ratio
SNDR\textsubscript{p} Peak Signal-to-Noise-and-Distortion Ratio
SR Slew Rate
VLSI Very Large Scale of Integration
VGA Variable Gain Amplifier

Symbols

Physical

\( k \) Boltzmann's constant \((1.38 \times 10^{-23} \text{ J/K})\)
\( q \) Elementary charge \((1.60 \times 10^{-19} \text{ C})\)
\( T \) Absolute temperature

Definitions

\( \Delta \) Quantizer step size
\( \delta_1, \delta_2 \) Settling error during the sampling or integration phase
\( \gamma \) Excess noise factor
\( \phi_i \) \(i^{th}\) phase of a two phase non overlapping clocking scheme
\( \rho_1, \rho_2 \) Static error of an integrator during sampling or integration phase

\( \sigma_{\Delta T} \) Standard deviation of the clock-jitter

\( \tau_1, \tau_2 \) Time available to settle during sampling or integration phase

\( A \) Gain of the OTA

\( A_i \) Amplitude of the input signal

\( A_0 \) Nominal OTA gain

\( A_\beta, A_{VT} \) Current factor and threshold voltage mismatch parameters

\( B \) Number of bits in the quantizer

\( C_{eq,cl1}, C_{eq,cl2} \) Equivalent closed-loop load capacitance of the OTA during sampling or integration phase

\( C_{eq,ol1}, C_{eq,ol2} \) Equivalent open-loop load capacitance of the OTA during sampling or integration phase

\( C_S, C_l \) Sampling and integration capacitance

\( C_P \) Parasitic input capacitance of the OTA

\( C_L \) Load capacitance of the OTA

\( du \) Duty-cycle of the feedback pulse in a continuous-time \( \Delta \Sigma \) converter

\( e_q \) Quantization noise error in the time domain

\( E_{q,r} \) Quantization noise error of stage \( r \) in a cascaded topology

\( f_s, f_N \) Signal bandwidth and Nyquist rate (i.e. twice the signal bandwidth)

\( f_{de1}, f_{de2} \) Dominant closed-loop pole of the OTA during the integration phase in Hz

\( f_s \) Frequency of the input signal

\( f_s \) Sampling frequency

\( g_{m1}, g_0 \) Transistor or amplifier transconductance and output conductance

\( H \) Loop filter of the \( \Delta \Sigma \) converter

\( HD_2, HD_3 \) Second and third-order harmonic distortions

\( H_e, H_z \) Noise and signal transfer functions

\( k \) Quantizer gain

\( KP_n, KP_p \) Transconductance parameter of NMOS and PMOS transistor

\( L \) Channel length of a MOS transistor

\( n \) Order of the \( \Delta \Sigma \) converter

\( N_n, N_p \) Number of unit capacitances connected to \( -V_{\text{REF}} \) and \( V_{\text{REF}} \), respectively

\( N_q \) Quantization noise power

\( N_{nc} \) Total number of unit capacitances

\( P \) Power consumption

\( p_{cl1}, p_{cl2} \) Dominant closed-loop pole of the OTA during sampling or integration phase

\( OSR \) Oversampling Ratio of a \( \Delta \Sigma \) modulator

\( R_1, R_2 \) Resistance in the signal path during sampling or integration phase

\( R_N, R_P, R_{NP} \) Resistance of nMOS, pMOS and transmission gate

\( \text{SHD}_i \) Ratio of the signal to the \( i^{th} \) harmonic distortion component

\( \text{SNR}_{0.25} \) Signal-to-Noise Ratio for a relative input signal of 0.25

\( v_D, v_G, v_S \) Drain, gate and source voltage

\( v_{DB}, v_{DS}, v_{GS} \) Drain to bulk, drain to source and gate to source voltages
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{GST}$</td>
<td>Gate-source overdrive voltage, i.e. $V_{GS} - V_T$</td>
</tr>
<tr>
<td>$V_{REF}$</td>
<td>Reference voltage of a converter</td>
</tr>
<tr>
<td>$V_T, V_{Th}, V_{Tp}$</td>
<td>Threshold voltage of nMOS and pMOS</td>
</tr>
<tr>
<td>$W$</td>
<td>Channel width of a MOS transistor</td>
</tr>
</tbody>
</table>
Abstract

List of Symbols and Abbreviations

1 Introduction
   1.1 Motivation and Applications .............................................. 1
      1.1.1 Asymmetric Digital Subscriber Line (ADSL) ...................... 2
      1.1.2 Wideband Receiver ................................................... 4
   1.2 The Presented Work ....................................................... 4

2 Architecture Study of Delta-Sigma Converters
   2.1 Introduction ............................................................... 7
   2.2 Operation Principle of Delta-Sigma Converters ...................... 8
      2.2.1 Nyquist-Rate ADC ................................................... 8
      2.2.2 Oversampled ADC ................................................... 14
      2.2.3 Oversampling Combined with Noise-Shaping: a ΔΣ ADC .......... 18
      2.2.4 Definition of Performance Metrics for a ΔΣ ADC ............... 22
      2.2.5 Ideal Performance of a ΔΣ ADC ................................... 25
   2.3 Optimal Coefficients for ΔΣ Converters ................................ 29
      2.3.1 Single-Loop Topologies .............................................. 30
         2.3.1.1 First-Order ΔΣ Converters ...................................... 33
         2.3.1.2 Second-Order ΔΣ Converters .................................... 35
         2.3.1.3 Third-order ΔΣ Converters ..................................... 38
         2.3.1.4 Fourth and Higher-Order ΔΣ Converters ....................... 42
         2.3.1.5 Other Single-Loop Topologies .................................. 42
      2.3.2 Cascaded Topologies .................................................. 43
   2.4 Performance Comparison of ΔΣ Topologies ............................ 53
   2.5 Continuous-Time Implementations ...................................... 56
   2.6 Linearity Issues of Multi-Bit ΔΣ Converters .......................... 61
      2.6.1 Trimming and Analog Calibration Techniques ..................... 67
      2.6.2 Digital Calibration Techniques ..................................... 68
      2.6.3 Dual-Quantization Techniques ...................................... 68
      2.6.3.1 Leslie-Singh Architecture ....................................... 69
2.6.3.2 Single-Loop Dual-Quantization Architecture .................. 71
2.6.3.3 Cascaded Dual-Quantization Architecture .................. 73
2.6.4 Dynamic Element Matching Techniques .......................... 74
  2.6.4.1 Randomization ........................................... 77
  2.6.4.2 Clocked Averaging (CLA) ................................ 79
  2.6.4.3 Individual Level Averaging (ILA) .......................... 81
  2.6.4.4 Data Weighted Averaging (DWA) .......................... 81
  2.6.4.5 Bi-directional Data Weighted Averaging (biDWA) ........... 86
  2.6.4.6 Partitioned Data Weighted Averaging (PDWA) ............... 88
  2.6.4.7 Data Directed Scrambling (DDS) .......................... 88
  2.6.4.8 Second-Order Data Weighted Averaging (DWA 02) .......... 91
  2.6.4.9 Vector-Quantizer Structures .............................. 92
2.6.4.10 Noise-Shaped DEM with Tree-Structures ...................... 94
2.6.4.11 Comparison ................................................. 96

2.7 Conclusion ............................................................. 96

3 Design Considerations for Multi-Bit ΔΣ Converters .................. 99
  3.1 Introduction ....................................................... 99
  3.2 Clock-Jitter ....................................................... 100
    3.2.1 Nyquist-Rate AD Converters .................................. 100
    3.2.2 Discrete-Time ΔΣ Converters ................................. 100
    3.2.3 Continuous-Time ΔΣ converters ................................ 101
    3.2.4 Comparison ................................................... 104
  3.3 Discrete-Time versus Continuous-Time ΔΣ Converters .............. 105
  3.4 System Level Considerations ..................................... 108
    3.4.1 Single Ended versus Differential Implementations ............ 108
    3.4.2 Implementations of Integrators with Single-Bit and Multi-Bit Feedback .................................................. 109
    3.4.3 Signal Swings .................................................. 112
  3.5 Non-Ideal Switched-Capacitor Integrator ............................ 112
    3.5.1 Finite Gain of the OTA ....................................... 115
    3.5.2 Dominant Closed-Loop Pole of the OTA ....................... 117
    3.5.3 Switch Resistance and Dominant Closed-Loop Pole of the OTA . 119
    3.5.4 Slew-Rate and Dominant Closed-Loop Pole of the OTA .......... 122
    3.5.5 Full Model Including Switch Resistance, Slew-Rate and Dominant Closed-Loop Pole ........................................ 126
  3.6 Other Non-Idealities in a Switched-Capacitor Integrator ........ 128
    3.6.1 Clock Feedthrough and Charge Injection ...................... 129
    3.6.2 Coefficient Mismatch .......................................... 130
    3.6.3 Non-Linear Capacitances ..................................... 130
    3.6.4 Non-Linear OTA Gain .......................................... 133
    3.6.5 Non-Linear Switch Resistance ................................ 135
  3.7 Non-Idealities of the DAC and the Quantizer ................. 141
    3.7.1 Non-Idealities of the DAC .................................... 141
### Contents

3.7.2 Non-Idealities of the Quantizer ........................................ 142
3.8 Noise Analysis ................................................................. 143
    3.8.1 Noise Contribution of the Different Integrators .................. 144
    3.8.2 Equivalent Input Noise of a Switched-Capacitor Integrator ........ 145
3.9 Power Estimation and Design Considerations .......................... 149
3.10 Conclusion ...................................................................... 158

4 Implementations ................................................................. 159
  4.1 Introduction .................................................................. 159
  4.2 A 15-bit 2.2MS/s 3.3V Cascaded ΔΣ Converter ..................... 159
    4.2.1 Topology Selection and System Level Design ................. 160
    4.2.2 Circuit Level Design .................................................. 165
      4.2.2.1 Design of the Integrator ...................................... 165
      4.2.2.2 Design of the Quantizer ....................................... 169
      4.2.2.3 Design of the Clock Generator ............................... 171
    4.2.3 Layout and Measurement Results ................................ 172
  4.3 A 16-bit 2.5 MS/s 5V Multi-Bit ΔΣ Converter .................... 176
    4.3.1 Topology Selection and System Level Design ................. 176
    4.3.2 Circuit Level Design .................................................. 178
      4.3.2.1 Implementation of the Data Weighted Averaging Algorithm 180
      4.3.2.2 Design of the Quantizer ....................................... 182
      4.3.2.3 Design of the DAC and the Integrator .................... 184
    4.3.3 Layout and Measurement Results ................................ 190
  4.4 Performance Comparison .................................................. 195
  4.5 Conclusion ...................................................................... 199

5 Conclusions ........................................................................ 201

A A Switched-Capacitor Integrator Including Slew-Rate Effects ........ 203
  A.1 Charges on the Capacitors .............................................. 204
  A.2 Calculations for the Sampling Phase ................................. 205
    A.2.1 Linear Settling ......................................................... 206
    A.2.2 Slewing during an Entire Clock Phase .......................... 206
    A.2.3 Slewing followed by Linear Settling ............................ 207
  A.3 Calculations for the Integration Phase ............................... 207
    A.3.1 Linear Settling ......................................................... 208
    A.3.2 Slewing during an Entire Clock Phase .......................... 208
    A.3.3 Slewing followed by Linear Settling ............................ 209
  A.4 Conclusion ...................................................................... 209

Bibliography .......................................................................... 211

Index .................................................................................... 223