RAPID PROTOTYPING OF DIGITAL SYSTEMS
Second Edition

A Tutorial Approach

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PREFACE

Changes to the Second Edition

The second edition of the text now includes Altera's 10.1 student edition software which adds support for Windows 2000 and designs that are three times larger using the new 70,000 gate UP 1X board. All designs in the book's CDROM have been updated to work with the original UP 1 board or the newer UP 1X board using the new Altera student version software. A coupon is included with the text for purchase of the new UP 1X board. The additional logic and memory in the UP 1X's FLEX 10K70 is useful on larger design projects such as computers and video games.

In addition to the new software, the second edition includes an updated chapter on programmable logic, new robot sensors and projects, optional Verilog examples, and a meta assembler which can be used to develop assembly language programs for the computer designs in Chapters 8 and 13.

Intended Audience

This text is intended to provide an exciting and challenging laboratory component for an undergraduate digital logic design class. The more advanced topics and exercises are also appropriate for consideration at schools that have an upper level course in digital logic or programmable logic. There are a number of excellent texts on digital logic design. For the most part, these texts do not include or fully integrate modern CAD tools, logic simulation, logic synthesis using hardware description languages, design hierarchy, and current generation field programmable logic device (FPLD) technology. The goal of this text is to introduce these topics in the laboratory portion of the course.

Design engineers working in industry may also want to consider this text for a rapid introduction to FPLD technology and logic synthesis using commercial CAD tools, if they have not had previous experience with this new and rapidly evolving technology.

Two tutorials on the Altera CAD tool environment, an overview of programmable logic, and a design library with several easy to use input and output functions were developed for this text to help students get started quickly. Early design examples use schematic capture and library components. VHDL is used for more complex designs after a short introduction to VHDL based synthesis.

The approach used in the text more accurately reflects contemporary practice in industry than the more traditional TTL protoboard based laboratory courses. With modern logic synthesis tools and large FPLDs, more advanced designs are needed to present challenging laboratory projects. Rather than being limited to a few TTL chips that will fit on a small protoboard, designs containing tens of thousands of gates are possible even with student versions of the CAD tools

and the UP 1 board. Even student laboratory projects can now implement entire digital systems.

Over the past three years, we have developed a number of interesting and challenging laboratory projects involving serial communications, state machines with video output, video games and graphics, simple computers, keyboard and mouse interfaces, robotics, and pipelined RISC processor cores.

Source files and additional example files are available on the CDROM for all designs presented in the text. The student version of the PC based CAD tool on the CDROM can be freely distributed to students. Students can purchase their own UP 1 board for little more than the price of a contemporary textbook. As an alternative, a few of the low-cost UP 1 or UP 1X boards can be shared among students in a laboratory. Course instructors should contact the Altera University Program for detailed information on obtaining student versions of the CAD tools and UP 1 boards for student laboratories.

Topic Selection and Organization

Chapter 1 is a short CAD tool tutorial that covers design entry, simulation, and hardware implementation using an FPLD. The majority of students can enter the design, simulate, and have the design successfully running on the UP 1 board in less than thirty minutes. After working through the tutorial and becoming familiar with the process, similar designs can be accomplished in less than 10 minutes.

Chapter 2 provides an overview of the UP 1 and UP 1X FPLD development boards. The features of the boards are briefly described. Several tables listing pin connections of various I/O devices serve as an essential reference whenever a hardware design is implemented on the UP 1 board.

Chapter 3 is an introduction to programmable logic technology. The capabilities and internal architectures of the most popular CPLDs and FPGAs are described. These include the MAX 7000 and FLEX 10K family CPLDs used on the UP 1 board, and the Xilinx 4000 family FPGAs.

Chapter 4 is a short CAD tool tutorial that serves as both a hierarchical and sequential design example. A counter is clocked by a pushbutton and the output is displayed in the seven-segment LED's. The design is downloaded to the UP 1 board and some real world timing issues arising with switch contact bounce are resolved. It uses several functions from the UP1core library which greatly simplify use of the UP 1's input and output capabilities.

Chapter 5 describes the available UP1core library I/O functions. The I/O devices include switches, seven-segment LED's, a multiple output clock divider, VGA output, keyboard input, and mouse input.

Chapter 6 is an introduction to the use of VHDL for the synthesis of digital hardware. Rather than a lengthy description of syntax details, models of the commonly used digital hardware devices are developed and presented. Most VHDL textbooks use models developed for simulation only and they frequently use language features not supported in synthesis tools. Our easy to understand synthesis examples were developed and tested using the Altera VHDL CAD tools.

Chapter 7 is a state machine design example. The state machine controls a virtual electric train system simulation with video output generated directly by the CPLD. Using track sensor input, students must control two trains and three track switches to avoid collisions.

Chapter 8 develops a model of a simple computer. The fetch, decode, and execute cycle is introduced and a brief model of the computer is developed using VHDL. A short assembly language program can be entered in the FPLD's internal memory and executed in the simulator.

Chapter 9 describes how to design an FPLD-based digital system to output VGA video. Numerous design examples are presented containing video with both text and graphics. Fundamental design issues in writing simple video games and graphics using the UP 1 board are examined.

Chapter 10 describes the PS/2 keyboard operation and presents interface examples for integration in designs on the UP 1 board. Keyboard scan code tables, commands, status codes, and the serial communications protocol are included. VHDL code for a keyboard interface is also presented.

Chapter 11 describes the PS/2 mouse operation and presents interface examples for integration in designs on the UP 1 board. Commands, data packet formats, and PS/2 serial communications protocols are included.

Chapter 12 develops a design for an adaptable mobile robot using the UP 1 board. Servo motors and several sensor technologies for a low cost mobile robot are described. A sample servo driver design is presented. Commercially available parts to construct the robot described in Chapter 12 can be obtained for around $50. Several robots can be built for use in the laboratory. Students with their own UP 1 board may choose to build their own robot following the detailed instructions found in section 12.6.

Chapter 13 describes a single clock cycle model of the MIPS RISC processor based on the hardware implementation presented in the widely used Patterson and Hennessy textbook, *Computer Organization and Design The Hardware/Software Interface.* Laboratory exercises that add new instructions, features, and pipelining are included at the end of the chapter.

We anticipate that many schools will still choose to begin with TTL designs on a small protoboard for the first few labs. The first chapter can also be started at this time since only OR and a NOT logic functions are used to introduce the CAD tool environment. The CAD tool can also be used for simulation of TTL labs, since an extensive TTL parts library is included with the student version.

Even though VHDL is a complex language, we have found after several years of experimentation that students can write VHDL to synthesize hardware designs after a short overview with a few basic hardware design examples. The use of VHDL templates and online help files in the CAD tool makes this process easier. After the initial experience with VHDL synthesis, students dislike the use of schematic capture on larger designs since it can be very time consuming. Experience in industry has been much the same since huge productivity gains have been achieved using HDL based synthesis tools for application specific integrated circuits (ASICs) and FPLDs.

Most digital logic classes include a simple computer design such as the one presented in Chapter 8 or a RISC processor such as the one presented in Chapter 13. If this is not covered in the first digital logic course, it could be used as a lab component for a subsequent computer architecture class.

A typical quarter or semester length course could not cover all of the topics presented. The material presented in Chapters 7 through 13 can be used on a selective basis. The keyboard and mouse are supported by UP1core library functions, and the material presented in Chapters 10 and 11 is not required to use these library functions for keyboard or mouse input. Information on video generation, PS/2 keyboard, and mouse interfacing is not readily available elsewhere.

A video game based on the material in Chapter 9 can serve as the basis for a team design project. For a final team design project, we use robots with sensors from chapter 12 that are controlled by the simple computer in chapter 8. The meta assembler in Appendix D is used to assemble the programs. Our students really enjoyed working with the robot described in Chapter 12, and it presents almost infinite possibilities for an exciting design competition.

Software and Hardware Packages

The new student version of Altera's MAX+PLUS II CAD tool is included with this book. UP 1 and UP 1X boards are available from Altera at special student pricing. A board can be shared among several students in a lab, or some students may wish to purchase their own board. Details and suggestions for additional cables and power supplies that may be required for a laboratory setup can be found in Section 2.5. Source files for all designs presented in the text are available on the CDROM.

Additional Web Material and Resources

There is a web site for the text with additional course materials, slides, text errata, and software updates at:

http://www.ece.gatech.edu/users/hamblen/book/bookse.htm

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