Appendix I  
Synthesizable and Non-Synthesizable Verilog Constructs

The list of synthesizable and non-synthesizable Verilog constructs is tabulated in the following Table.

<table>
<thead>
<tr>
<th>Verilog Constructs</th>
<th>Used for</th>
<th>Synthesizable construct</th>
<th>Non-Synthesizable Construct</th>
</tr>
</thead>
<tbody>
<tr>
<td>module</td>
<td>The code inside the module and the endmodule consists of the declarations and functionality of the design</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Instantiation</td>
<td>If the module is synthesizable then the instantiation is also synthesizable</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>initial</td>
<td>Used in the test benches</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>always</td>
<td>Procedural block with the reg type assignment on LHS side. The block is sensitive to the events</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>assign</td>
<td>Continuous assignment with wire data type for modeling the combinational logic</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>primitives</td>
<td>UDP’s are non-synthesizable whereas other Verilog primitives are synthesizable</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>force and release</td>
<td>These are used in test benches and non-synthesizable</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>delays</td>
<td>Used in the test benches and synthesis tool ignores the delays</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>fork and join</td>
<td>Used during simulation</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>ports</td>
<td>Used to indicate the direction, input, output and inout. The input is used at the top module</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>parameter</td>
<td>Used to make the design more generic</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>time</td>
<td>Not supported for the synthesis</td>
<td>No</td>
<td>Yes</td>
</tr>
</tbody>
</table>

(continued)
## Appendix I: Synthesizable and Non-Synthesizable Verilog Constructs

<p>| | | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>real</strong></td>
<td>Not supported for synthesis</td>
<td>No</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td><strong>functions and task</strong></td>
<td>Both are synthesizable. Provided that the task does not have the timing constructs</td>
<td>Yes</td>
<td>No</td>
<td></td>
</tr>
<tr>
<td><strong>loop</strong></td>
<td>The for loop is synthesizable and used for the multiple iterations.</td>
<td>Yes</td>
<td>No</td>
<td></td>
</tr>
<tr>
<td><strong>Verilog Operators</strong></td>
<td>Used for arithmetic, bitwise, unary, logical, relational etc are synthesizable</td>
<td>Yes</td>
<td>No</td>
<td></td>
</tr>
<tr>
<td><strong>Blocking and non-blocking assignments</strong></td>
<td>Used to describe the combinational and sequential design functionality respectively</td>
<td>Yes</td>
<td>No</td>
<td></td>
</tr>
<tr>
<td><strong>if-else, case, case x, case z</strong></td>
<td>These are used to describe the design functionality depending on the priority and parallel hardware requirements</td>
<td>Yes</td>
<td>No</td>
<td></td>
</tr>
<tr>
<td><strong>Compiler directives</strong> (‘ifdef,’‘undef,’‘define’)</td>
<td>Used during synthesis</td>
<td>Yes</td>
<td>No</td>
<td></td>
</tr>
<tr>
<td><strong>Bits and part select</strong></td>
<td>It is synthesizable and used for the bit or part select</td>
<td>Yes</td>
<td>No</td>
<td></td>
</tr>
</tbody>
</table>
Appendix II
Xilinx Spartan Devices

- Xilinx Spartan 3 Devices

<table>
<thead>
<tr>
<th>Device</th>
<th>System Gates</th>
<th>Equivalent Logic Cells</th>
<th>CLB Array (One CLB = Four Slices)</th>
<th>Distributed RAM Bits (K=1024)</th>
<th>Block RAM Bits (K=1024)</th>
<th>Dedicated Multipliers</th>
<th>DCMs</th>
<th>Max. User I/O</th>
<th>Maximum Differential I/O Pairs</th>
</tr>
</thead>
<tbody>
<tr>
<td>XC3S250</td>
<td>50K</td>
<td>1,728</td>
<td>16 12 192</td>
<td>12K</td>
<td>72K</td>
<td>4</td>
<td>2</td>
<td>124</td>
<td>56</td>
</tr>
<tr>
<td>XC3S200</td>
<td>200K</td>
<td>4,320</td>
<td>24 20 480</td>
<td>30K</td>
<td>216K</td>
<td>12</td>
<td>4</td>
<td>173</td>
<td>76</td>
</tr>
<tr>
<td>XC3S400</td>
<td>400K</td>
<td>8,064</td>
<td>32 28 896</td>
<td>56K</td>
<td>288K</td>
<td>16</td>
<td>4</td>
<td>204</td>
<td>116</td>
</tr>
<tr>
<td>XC3S600</td>
<td>1M</td>
<td>17,280</td>
<td>48 40 1,920</td>
<td>120K</td>
<td>432K</td>
<td>24</td>
<td>4</td>
<td>301</td>
<td>175</td>
</tr>
<tr>
<td>XC3S1500</td>
<td>1.5M</td>
<td>29,952</td>
<td>64 52 3,538</td>
<td>268K</td>
<td>576K</td>
<td>32</td>
<td>4</td>
<td>467</td>
<td>221</td>
</tr>
<tr>
<td>XC3S2000</td>
<td>2M</td>
<td>48,060</td>
<td>80 64 5,120</td>
<td>320K</td>
<td>720K</td>
<td>40</td>
<td>4</td>
<td>555</td>
<td>270</td>
</tr>
<tr>
<td>XC3S4000</td>
<td>4M</td>
<td>92,208</td>
<td>96 72 6,912</td>
<td>422K</td>
<td>1,728K</td>
<td>96</td>
<td>4</td>
<td>633</td>
<td>300</td>
</tr>
<tr>
<td>XC3S6000</td>
<td>6M</td>
<td>148,944</td>
<td>120 80 8,320</td>
<td>520K</td>
<td>1,872K</td>
<td>104</td>
<td>4</td>
<td>633</td>
<td>300</td>
</tr>
</tbody>
</table>

Notes:
1. Logic Cell a 4-input Look-Up Table (LUT) plus a 'D' flip-flop. "Equivalent Logic Cells" equals "Total CLBs" x 8 Logic Cells/CLB x 1.125 effectiveness.
2. These devices are available in Xilinx Automotive version as described in DS314: Spartan-3 Automotive XA FPGA Family.
• Spartan 3 Family Architecture

Notes:
1. The two additional block RAM columns of the XC3S4000 and XC3S5000 devices are shown with dashed lines. The XC3S50 has only the block RAM column on the far left.

• Xilinx Spartan 3 Package information for Part no XC3S400-4PQ208C
Appendix II: Xilinx Spartan Devices

For more information please use the following link http://www.xilinx.com/support/documentation/data_sheets/ds099.pdf.

- Xilinx FPGA Spartan 3E Devices

<table>
<thead>
<tr>
<th>Device</th>
<th>System Gates</th>
<th>Equivalent Logic Cells</th>
<th>CLBs Array (One CLB = Four Slices)</th>
<th>Distributed RAM bits (^1)</th>
<th>Block RAM bits (^1)</th>
<th>Dedicated Multipliers</th>
<th>DCMs</th>
<th>Maximum User I/O</th>
<th>Maximum Differential I/O Pairs</th>
</tr>
</thead>
<tbody>
<tr>
<td>XC3S100E</td>
<td>100K</td>
<td>2.190</td>
<td>22 16 240 960</td>
<td>15K</td>
<td>72K</td>
<td>4</td>
<td>2</td>
<td>10K</td>
<td>40</td>
</tr>
<tr>
<td>XC3S250E</td>
<td>250K</td>
<td>5.509</td>
<td>34 26 512 2,448</td>
<td>38K</td>
<td>22K</td>
<td>12</td>
<td>4</td>
<td>172</td>
<td>60</td>
</tr>
<tr>
<td>XC3S500E</td>
<td>500K</td>
<td>10,076</td>
<td>46 34 1,164 4,856</td>
<td>79K</td>
<td>38K</td>
<td>20</td>
<td>4</td>
<td>232</td>
<td>92</td>
</tr>
<tr>
<td>XC3S1200E</td>
<td>1,200K</td>
<td>19,512</td>
<td>60 46 2,160 8,672</td>
<td>126K</td>
<td>50K</td>
<td>28</td>
<td>8</td>
<td>304</td>
<td>124</td>
</tr>
<tr>
<td>XC3S1600E</td>
<td>1,600K</td>
<td>33,192</td>
<td>76 58 3,088 14,752</td>
<td>231K</td>
<td>64K</td>
<td>56</td>
<td>8</td>
<td>376</td>
<td>156</td>
</tr>
</tbody>
</table>

Notes:
1. By convention, one Kb is equivalent to 1,024 bits.

- Xilinx Spartan 3E Architecture
- Xilinx Spartan 3E package information

For more information please use the following link http://www.xilinx.com/support/documentation/data_sheets/ds312.pdf.
Appendix III
Design For Testability

The Design For Testability (DFT) and its necessity is discussed in summarized.

In the practical ASIC design, the DFT is used to find out various kinds of faults in the design. For FPGA designs this step is excluded. The necessity of DFT is for early detection of the faults in the design using scan chain insertions. The functional abstraction of defects is called as fault and the abstraction of the fault is the system level error. Physical testing is carried out after manufacturing of chip to understand the fabrication-related issues or faults.

The defects in the design can be physical or electrical. Physical defects are due to silicon or defective oxide. Electrical defects are short, open, transistor defects and changes in the threshold voltage.

Few of the faults in the design are following

1. Stuck at faults: Stuck at one or Stuck at zero
2. Memory faults or pattern-sensitive faults
3. Bridging faults
4. Cross point faults
5. Delay faults

Testing process is the process of test pattern generation, test pattern application and output evaluation.

Generally, the test flow includes the following:

1. Identify the target faults
2. Test generation
3. Fault Simulation
4. Testability
5. DFT

- Design For Testability (DFT)
  The DFT is required to reduce the defect level in the design. Consider the following design; in this design it is not possible to give the test input so design is not testable. The DFT uses the concept of controllability and observability.
  The key steps are
1. RTL design
2. Simulation
3. Synthesis
4. Insert scan chain
5. Layout

If every data input of the register need to be forced to the known value during the test, then the design is controllable.

Observability indicates the ability to observe the node at primary output. The design needs to be controllable and observable.

As shown in the following design, the design input of comb_logic1 is controllable and the output from comb_logic3 is observable. But comb_logic1 and comb_logic2 are not observable. So for detection of faults, it is essential to make comb_logic1, comb_logic2, and comb_logic3 controllable as well as observable.

- The basic DFT techniques are: Ad-HOC DFT and Structured DFT. The structured DFT includes the scan-based DFT which is again classified as MUX-based DFT and level-sensitive, element-based DFT. Another structured DFT technique is MBIST and LBIST. JTAG is used for boundary scan.

Basic MUX-based technique is described below.

- MUX-based scan cell
The MUX-based scan cell is shown below and it has additional inputs as Test_data, Scan_en. The MUX is inserted at the input of the D flip-flop and during testing Scan_en=1 the D input is Test_data. During normal operation, the Scan_en=0 and Data_in can pass through the combinational logic to the D input. Thus, the following cell works both in the test and normal modes. The clk can be scan_clk during the test mode.
MUX-based scan chain:

Normally used method is insertion of scan by using MUX logic. MUX-based scan cell shown in the above figure is used to replace the sequential elements from the design. Depending on the requirements the design team decides whether to use partial scan method or full scan method. In the partial scan method few of the sequential elements are replaced by the MUX based scan cell. In the full scan method, all the sequential elements are replaced by the MUX-based scan cell. Due to scan insertion, the area and timing of the design has significant impact. Scan insertion increases the area of the design and due to added MUX-based logic even it affects on the timing of the design. The following example shows the scan chain using MUX-based scan cells. Most of the time, the partial scan is recommended if area and timing is the constraint but this reduces overall fault coverage. If full scan is used then it increases area and has significant impact on timing but this improves overall fault coverage.
Scan Design rules

Following are few of the scan design rules need to be considered:

1. Generated clocks in the design: There should not be generated clocks in the design as they are not controllable.
2. Combinational feedback loop: There should not be any combinational loop in the design as it creates issues in the timing analysis and hence it is essential to break the combinational loop.
3. Gated clocks: Gated clocks need to be avoided as they are not controllable.
4. Asynchronous Control signals: There should not be any internally generated asynchronous control signals.
5. Do not mix the positive and negative edge triggered flip-flops.
6. Avoid use of latches in the design.
7. If shift registers are used then do not replace them by using scan enabled flip-flops but only ensure the enable control.
8. Do not use the clock input as data.
9. Bypass the memories during DFT.
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