Index

A
Agilent N5247A PNA-X network analyzer, 48
Analog-to-digital converter (ADC), 7, 105

B
Backscattering technique, 8

C
Cadence Virtuoso Spectre circuit simulator, 31
Complementary metal oxide semiconductor (CMOS) technology, 2–3
40 nm technology
  cascode structure, 113–114
  current density, 107–108
  gain match, 110–112
  measurement result, 114–116
  specifications, 109–110
  topology selection, 108–109
low average power dissipation, 133–134
on-chip antenna integration, 133
phased-array architecture, 134
rectifiers, 133
65-nm technology
  Dickson structure, 50–51
  measured output voltage, 53
  measured S_{11}, 52–53
  micrograph, 51–52
  schematic of, 51

D
Duplex system, 23–25
Duty-cycle factor (DCF), 8

E
Electromagnetic (EM) software, 51
End-of-burst monitor (EBM), 64
Energy models
  antenna and matching network, 81–82
  LNA, 83–84
  RF signal, 82–83
  self-mixer, 84–85
  system limitations, 85–86
Error vector magnitude (EVM), 107

F
Full-wave rectifier, 21–22

H
Half-wave rectifier, 21–22
High-frequency (HF) bands, 1

I
Impulse radio ultra-wideband (IR-UWB), 7
Industrial-scientific-medical (ISM) bands, 1
Injection-locked oscillator (IJLO), 81, 84–85

L
Low-frequency (LF) bands, 1
Low noise amplifier (LNA)
  incoming signal, 81
  single-stage, 83–84
  60 GHz
    cascaded two-stage cascode structure, 92–93, 113–114
Low noise amplifier (LNA) (cont.)
  design, 90–91
  gain match, 110–112
  gate resistance, 91
  measurement result, 114–116
  parameter $k$, 92
  power consumption, 91–92
  specifications, 109–110
  technology, 107–108
  topology selection, 108–109
Low power consumption
  backscattering technique, 8
  IR-UWB, 7
  super-regenerative architecture, 7–8
  WuRx architecture, 8

M
Millimeter wave identification (MMID), 1–2
mm-wave rectifier, 3
  comparison of, 56–57
  50–60 GHz broadband rectifier
    measured efficiency, 55, 56
    measured output DC voltage vs. input
      RF power characteristic, 54–55
    measured $S_{11}$, 54–55
    measured sensitivity, 54, 56
    micrograph, 53–54
  inductor peaking, 45–46
  mechanisms, 43–44
multi-stage inductor-peaked rectifier
  Dickson structure, 50–51
  measured output voltage, 53
  measured $S_{11}$, 52–53
  micrograph, 51–52
  schematic of, 51
output filter, 46–47
single-stage inductor-peaked rectifier
  input voltage $V_{in}$, 48
  measured efficiency, 49–50
  measured output voltage, 48–50
  micrograph, 47–49
  on-wafer RF and DC probes, 48
  $S_{11}$ measurement, 48–49
threshold voltage modulation, 44–45
mm-wave temperature sensor nodes
  EBM, 64
  multi-stage rectifier, 63
  on-chip antenna
    matching, 67–68
    slab waveguide, 66
    TE mode, 66–68
  TM mode, 66–68
    zero Hz cut-off frequency, 66
    with one antenna, 32, 73–76
    performance, 75, 77
    RF switch, 64–66
    system description, 60–61
    temperature sensing, 69–70
    with two antennas
      architecture, 61–62
      environment temperature, 71, 75
      fully wireless node, 70–71
      measured efficiency, 71–72
      measured sensitivity, 71–72
      micrograph, 71
      tag charging and discharging, 71, 74
      ultra-low-power transmitter, 71, 73
mm-wave ultra-low-power receiver
  energy models
    antenna and matching network, 81–82
    LNA, 83–84
    RF signal, 82–83
    self-mixer, 84–85
    system limitations, 85–86
    evaluation, 86–87
    passive mixer, 93–94
    RTRx, 80–81
  60 GHz injection-locked oscillator
    current-reuse cascade topology, 88–89
    locking range, 90
    methods, 88–89
    phase shift, 89–90
    schematic of, 90, 91
  60 GHz low power differential LNA
    cascaded two-stage cascode structure, 92–93
    design, 90–91
    gate resistance, 91
    parameter $k$, 92
    power consumption, 91–92
  60 GHz OOK receiver
    chip photo, 95–96
    down-converting, 95, 97
    measured data stream, 97, 98
    measured IF spectrum, 95–96
    performance, 98
mm-wave wirelessly powered sensor node
  system, see Power REDuced MonolithIc Sensor System (PREMISS) system
mm-wave wireless power transfer, 7
Monolithic wireless sensor system, 2–3
Multi-stage rectifier, 23, 34
- inductor-peaked
  - Dickson structure, 50–51
  - measured output voltage, 53
  - measured $S_{11}$, 52–53
  - micrograph, 51–52
  - schematic of, 51
- mm-wave temperature sensor nodes, 63

Power REduced Monolithic Sensor System (PREMISS) system, 3
- block diagram, 14
- link budget calculation
  - downlink, 15–17
  - uplink, 17–19
- system architecture, 13–14

N
Noise factor (NF), 83–84

O
On-Off-Keying (OOK) receiver, 81, 84
- chip photo, 95–96
- down-converting, 95, 97
- measured data stream, 97, 98
- measured IF spectrum, 95–96
- performance, 98

P
Phased-array systems
- advantages, 102–104
- 5-bit switch-type phase shifter
  - broadband phase difference characteristic, 122
  - chip photo, 125–126
  - CMOS switches, 123–124
  - directional high gain antennas, 115
  - insertion phase, 121–122
  - measured insertion phase, 126
  - measured relative phase shift, 126–127
  - performance, 128, 130
  - phase difference, 122–123
  - phase shift realization, 116–120
  - RMS gain errors, 127, 129
  - RMS phase errors, 127, 129
  - schematic of, 125
  - stage sequence, 124–125
  - 32 phase settings, 127–128
  - working mechanism, 121–122
- link budget, 101–102
- receiver front-end, 105–107
- signal path, 104–105
- 60 GHz LNA
  - cascode structure, 113–114
  - gain match, 110–112
  - measurement result, 114–116
  - specifications, 109–110
  - technology, 107–108
  - topology selection, 108–109
- system architecture, 101–102

R
Radio frequency identification (RFID) system
- LF and HF bands, 1
- MMID, 1–2
- tag system, 24
- UHF and ISM bands, 1

Rectifier
- challenges, 38–40
- high input power
  - efficiency and input voltage, 37
  - efficiency and threshold voltage, 36
  - input referred capacitance, 33
  - maximum efficiency, 35–36
  - MOS transistor, 34
  - $N$-stage multi-stage rectifiers, 33
  - overlap and junction capacitance, 33–34
  - power dissipation, 34
  - $W/L$ ratio, 35
- limitation, 37–38
- low input power
  - assumptions, 27
  - equilibrium voltage, 28–29
  - input resistance, 29–30
  - simulation results, 31–33
  - single-stage rectifier, 26
  - SPICE model, 26–27
  - storage capacitor charging, 30–31
  - time varying voltage, 27
- performance parameters
  - architecture, 23–24
  - efficiency, 24–25
  - sensitivity, 24–25
  - structure, 21–23
  - subthreshold region, 25

S
Sequential system, 23–25
Signal to noise ratio (SNR), 86–87
Single-pole single-throw (SPST) RF switch, 65–66
Single-stage rectifier
- Cadence Virtuoso Spectre circuit simulator, 31
Single-stage rectifier (cont.)
equivalent small-signal (AC signal) model, 26
  inductor-peaked
    input voltage $V_{in}$, 48
    measured efficiency, 49–50
    measured output voltage, 48–50
    micrograph, 47–49
    on-wafer RF and DC probes, 48
    $S_{11}$ measurement, 48–49
  optimization, 34
Single-stage T-type switched phase shifter
  broadband phase difference characteristic, 122
    chip photo, 125–126
    CMOS switches, 123–124
    directional high gain antennas, 115
    insertion phase, 121–122
    measured insertion phase, 126
    measured relative phase shift, 126–127
    performance, 128, 130
    phase difference, 122–123
    phase shift realization, 116–120
    RMS gain errors, 127, 129
    RMS phase errors, 127, 129
    schematic of, 125
    stage sequence, 124–125
    32 phase settings, 127–128
    working mechanism, 121–122
Super-regenerative architecture, 7–8

T
  Third-order input intercept point (IIP$_3$), 83–84
  Transverse electric (TE) mode, 66–67
  Transverse magnetic (TM) mode, 66–67

U
  Ultra-high-frequency (UHF) bands, 1

V
  Variable-gain-amplifier (VGA), 105–106
  Voltage controller oscillator (VCO), 18

W
  Wake-up receiver (WuRx) architecture, 8
  Wireless power transfer (WPT), 3
    electrical coupling, 6
    inductive coupling, 6
    rectifier performance
      architecture, 23–24
      efficiency, 24–25
      sensitivity, 24–25
    RF energy transfer, 6
    state-of-the-art receivers, 97
    system description, 60–61
  Wireless sensor networks (WSNs), 8–9