# Index

## A
- ARM processors, 199, 202
- Availability, 1

## B
- Backward tracing algorithm, 52
- Binary search, 153

## C
- Causal logging, 113, 114
- Checking
  - analysis of, 71
  - hardware, 68
  - system monitoring of, 83
- Checking, ERRIC processor, 208, 209
- Checking, system software, 63, 65
- Complexity, ERRIC processor, 210
- Configuration control (Hardware), 87, 96, 98
- Control, Data, Predicate model
  - (CDP) of program, 61
- Control structures, 59, 61
- Coverage of fault, 23, 31, 38–41
- CuriOS, 186

## D
- Data structures, 58–60
- Dependency matrix of a system, 45–48

## E
- EROS, 186
- ERRIC processor, 199, 202–204
- Efficiency of malfunction tolerance, ERRIC, 209

## F
- Efficiency of recovery, 147
- Essential recoverable reduced instruction computer (ERRIC), 189–192
- Failure rate, ERRIC processor, 209
- Fault tolerance (FT), 1–5, 12–14, 16, 18–21
- Fault tolerance as a process, 23
- Fault-tolerant interruption handler, 183
- Fault-tolerant run-time systems, 185
- Fault-tolerant scheduler, 184
- Forward tracing algorithm, 51, 53
- Functional tests, 68, 69, 103

## G
- Generalized algorithm of fault tolerance (GAFT), 23, 24, 26–28, 31, 34, 35
- Graceful degradation, 92, 98

## H
- Hardware faults, 7, 8, 10
- Hardware monitor, 183
- Hardware state diagram, 98, 99
- Hardware support for recovery point formation, 117
- Hardware syndrome, 67, 70, 88, 89

## I
- Informational redundancy, 15, 19
- Instruction set, 194
- Integrity OS, 185
- Intel processors, 199
Index

L
L4ReAnimator, 185
Language resources, 161, 176
Language support of recovery, 177
Linear search, 149

M
Main resources monitor, 183
Malfunctions, 7, 9
Malfunctions, ERRIC processor, 208, 210
Mean time to failure (MTTF), 11, 21
Minix 3, 186
Model of faults, 17, 18, 22
Model of fault tolerance, 17, 18
Modified Linear Recovery, 154
Modified Linear Recovery (MLR) Algorithm
Characteristics of, 138
in malfunction, 140
in multiple malfunction, 137
in permanent faults, 140
Module loader, 184
Monitor of testing, 184
Multiple bits upsets (MBU), 8, 9

N
nWhile loop, 61

O
Optimistic logging, 113, 114
Overheads, ERRIC processor, 207, 210

P
Performance, GAFT property, 31, 35
Permanent faults, ERRIC processor, 208, 209
Permanent hardware faults, 9
Pessimistic logging, 114
Preparation for recovery, system software, 66
Principle of Active System Control, 47
Principle of Active System Safety
(PASS), 47, 48, 51, 53
Procedure recovery, 116
Processor architecture, 189, 199, 200
Processor reliability, ERRIC, 207, 208
Programming languages, 160
activities, 161, 171, 181
message passing syntax, 161, 181

R
Real-time scheduling of testing
as a task, 67, 73
Reconfigurability, 3
Reconfiguration monitor, 183
Reconfiguration, system software, 65
Recovery
at instruction level, 136
at procedure level, 136
Recovery algorithms, 129
Recovery matrix (RM), 48, 50
Recovery preparation, 106–108
Recovery, system software, 66
Redundancy, 3
Redundancy, ERRIC processor, 208–210
Redundancy handling, 13, 14, 16, 20, 21
Reliability, 3, 11–14, 18, 21
Reliability, GAFT property, 31, 34, 35, 36
Resources management monitor, 183
Run-Time System Structure, 183

S
SPARC processor, 199, 202
Scalability, 3
Simplicity, 3
Single event upsets (SEU), 7–9
Sliding dropping diagnosis (SDD), 71
Sliding testing, 71
Structural redundancy, 15, 16
System diagnostic module, 184
System software (SSW), 1, 3–5, 57, 58, 62, 63
life cycle, 63, 64
life cycle versus fault tolerance, 63
phases, 65

T
Testing, 67, 69–73, 76, 77
asynchronous, 76, 103
extended, 79
of time-sharing systems, 79
Time redundancy, 15, 19, 21
Tolerance, 18