APPENDIX A

An Expandible Family of Cascade $\Sigma\Delta$ Modulators

Given the high signal bandwidths required in nowadays telecom applications, the oversampling ratio of $\Sigma\Delta$Ms must be restricted to low values in order to run the modulator at a feasible clock rate. Thus, high-order shaping and/or multi-bit quantization must be usually used in order to achieve the required modulator resolution. Among the variety of existing alternatives, the combination of both cascade $\Sigma\Delta$ architectures and dual-quantization techniques have proved to be a feasible and efficient approach to enhance the limited dynamic range attainable at low oversampling. These architectures circumvent the stability problems associated to high-order $\Sigma\Delta$ loops by cascading only 1st- and 2nd-order stages, whereas mechanisms for correcting the non-linearity of the multi-bit DAC can be avoided provided that multi-bit quantization is not used in the modulator front-end stage [Bran91b] [Mede99b] [Mori00] [Lamp01] [Rio01a] [Gupta02].

Further investigation of the potentialities of these architectures have led us to propose an easily expandible, modular family of high-order cascade $\Sigma\Delta$Ms. Thanks to a proper selection of the integrator coefficients, this family of cascades preserves a low systematic loss of resolution and a high overload level, regardless the overall modulator order.

A.1 Topology Description

Fig. A.1 shows the generic block diagram of the proposed family of high-order cascades, henceforth called 2$^{-1L-2}$ $\Sigma\Delta$M. An $L$th-order modulator is formed with a 2nd-order stage followed by $L-2$ identical 1st-order stages. As in all cascade $\Sigma\Delta$Ms, the outputs of the $L-1$ stages are combined and processed in the digital domain through simple operators to cancel out the quantization noise generated in each stage but the last one. Linear analysis shows that the output of the 2$^{-1L-2}$ $\Sigma\Delta$M can be expressed in the $z$-domain as

$$Y(z) = z^{-L}X(z) + 2(1 - z^{-1})^L E_N(z) \tag{A.1}$$
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where $X(z)$ stands for the input signal, which is simply delayed, and $E_n(z)$ stands for the last-stage quantization error, which is $L$th-order shaped. Note that the cascade response equals that of an ideal $L$th-order $\Sigma\Delta M$, except for the scaling factor 2. This factor derives from the signal scaling required to avoid premature overload when transmitting the signal from one stage to the next.

By integrating the error term in eq(A.1) over the signal band, the in-band quantization error power is obtained as

$$P_Q = 4\sigma_Q^2 \cdot \frac{\pi^{2L}}{(2L+1)OSR^{2L+1}}$$

where $\sigma_Q^2 = \Delta^2/12$ is the power associated to the quantization error in the last-stage single-bit quantizer ($\Delta = 2V_{ref}$ stands for its full scale). Note that the factor 2 in eq(A.1) quadruples the in-band quantization error power and, thus, leads to a reduction of 6dB (1bit) in the dynamic range of the $2^{-L-2}$ cascade in comparison with an ideal $L$th-order $\Sigma\Delta M$. This systematic loss of resolution is one of the smallest possible and considerably smaller than that of other high-order cascades [Feld98] [Miao98] [Mori00]. More importantly, it is constant, regardless of the number of stages.

In fact, the most appealing feature of this architecture—with the set of coefficients proposed—is that it can be easily set to any order, just by changing the number of identical 1st-order stages. As shown in Fig.A.2, a correct operation is maintained with constant overload level, regardless the overall modulator order.
A.1 Topology Description

The set of integrator coefficients depicted in Fig. A.1 presents also the following interesting properties:

- The output swing required in all integrators does not exceed the quantizer full scale. Such an appealing feature for low-voltage implementations is illustrated in Fig. A.3 for the 5th-order cascade.
- The largest coefficient of each three-weight integrator can be obtained as the summation of the others, so that three-branch SC integrators are not required. By proper sharing of the SC input stages, all coefficients can be implemented with just two-branch integrators, which minimizes the total number of unit capacitors.
- All 1st-order stages contain the same coefficients, so that they can be electrically identical. This considerably simplifies the electrical and physical implementation of the modulator.

FIGURE A.2 SNDR curves of the $2^{-1L-2}$ cascade for several modulator orders ($OSR = 16$).

FIGURE A.3 Histogram of the integrator outputs relative to the reference voltage for $L = 5$. 
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An Expandible Family of Cascade \( \Sigma \Delta \) Modulators

\[ \text{[Dias93]} \ [\text{[Tan93]} \text{ can be easily achieved in the } 2^{-L^{-2}} \text{ cascade } \Sigma \Delta \text{M by including multi-bit quantization only in the last stage, while the remaining are single-bit. This being the case, the coefficients in the last-stage integrator can be multiplied by a factor 2 in order to have a loop gain of 1 if the full scales of the multi-bit ADC and DAC coincide, what considerably simplifies their design.} \]

If errors in the multi-bit DAC are considered in the linear analysis, the output of the dual-quantization \( 2^{-L^{-2}} \Sigma \Delta \)M can be obtained as

\[ Y(z) = z^{-L}X(z) + 2(1 - z^{-1})^{L}E_{N}(z) + 2(1 - z^{-1})^{(L-1)}E_{D}(z) \]  \( \text{(A.3)} \)

where \( E_{D}(z) \) stands for the error of the last-stage multi-bit DAC in the \( z \)-domain, which is \( (L-1) \)-th-order shaped. Thus, provided that errors in the multi-bit DAC are considerably high-pass filtered, its non-linearity can be tolerated to some extent with no need for calibration/correction mechanisms.

The in-band quantization error power can be estimated as

\[ P_{Q} = 4\sigma_{Q}^{2} \frac{\pi^{2L}}{(2L + 1)OSR^{2L+1} + 4\sigma_{D}^{2}} \cdot \frac{\pi^{2(L-1)}}{(2L-1)OSR^{2L-1}} \]  \( \text{(A.4)} \)

with \( \sigma_{Q}^{2} = \frac{1}{12} \left( \frac{\Delta}{2^{B-1}} \right)^{2} \), \( \sigma_{D}^{2} \approx \frac{1}{2} \Delta^{2} \cdot \left( \frac{INL}{100} \right)^{2} \)

where \( \sigma_{Q}^{2} \) is the power of the last-stage quantization error (\( \Delta = 2V_{\text{ref}} \) stands for the multi-bit quantizer full scale and \( B \) for its resolution) and \( \sigma_{D}^{2} \) is the power associated to the DAC errors, with \( INL \) being the DAC integral non-linearity expressed in \%FS.
A.2 Non-Ideal Performance

As stated in Chapter 2, SC implementations of cascade modulators suffer from certain non-ideal behaviors more than their single-loop counterparts; namely, finite amplifier DC gain and capacitor mismatch. Both non-idealities modify the ideal integrator z-domain transfer function, thus altering the quantization error transfer function. Since this variation is not correlated to changes of the cancellation logic, mismatch appears between the analog and digital processing that precludes perfect cancellation of the low-order quantization errors.

Into first-order approximation, the in-band power of the error leakages is independent of \( L \), because they are generated in the modulator first stage, which is the same for whatever \( L \). Making use of equations (3.7), (3.12), and (3.13), it can be expressed as

\[
\Delta P_{Q}(\mu, \sigma_{e}) = \frac{\Delta^{2}}{12} \cdot \left( \frac{25}{16A_{DC}^{2}} \cdot \frac{\pi^{2}}{3OSR} + 36\sigma_{c}^{2} \cdot \frac{\pi^{4}}{5OSR^{3}} \right) \quad (A.5)
\]

where \( A_{DC} \) stands for the 1st-stage amplifier DC gain and \( \sigma_{c} \) is the capacitor standard deviation. Comparing equations (A.2) [or (A.4)] and (A.5) for a given \( OSR \), it is clear that for certain values of \( A_{DC}, \sigma_{c}, \) and \( L \), leakages may dominate the in-band error power, thus imposing an upper bound to the practical values of \( L \).

In order to estimate this limit under realistic circuit imperfections, Fig. A.5a shows the simulated half-scale \( SNDR \) as a function of the amplifier DC gain for \( OSR = 16 \). Fig. A.5b shows the \( SNDR \) histograms obtained from Monte Carlo behavioral simulation assuming 0.1\% sigma in capacitor ratios—0.05\% is currently featured by metal-insulator-metal (MiM) capacitors in CMOS processes. Under these conditions, mainly because of the matching sensitivity, the 7th-order architecture seems not worth implementing for \( OSR = 16 \). Nevertheless, the 6th-order modulator provides 90-dB worst-case \( SNDR \) with a DC gain of 2500. Specially robust is the 5th-order cascade requiring a DC gain of 1000 to achieve 80-dB worst-case \( SNDR \) for \( OSR = 16 \). It is important to remark that these gains are basically needed for the 1st-stage amplifiers. The DC-gain requirement for the integrators in the remaining \( L-2 \) stages of the cascade are much more relaxed. This is also applicable to other circuit imperfections such as electronic noise, finite dynamics, non-linearity, mismatch, etc. This practice allows us to use simpler circuit topologies and layouts for these stages, thus saving area and power consumption.

In the same way as the modulator order, in practice, the number of bits in the last-stage quantizer \( (B) \) cannot be arbitrarily large. As shown in Fig. A.6, for a given oversampling ratio, the evolution of the overall effective resolution with
FIGURE A.5 Effect of (a) finite DC gain and (b) capacitor mismatch on the SNDR of single-bit 2-1^L-2 \( \Sigma\Delta \)Ms for \( OSR = 16 \).

FIGURE A.6 ENOB of 2-1^{L-2} cascade \( \Sigma\Delta \)Ms versus the resolution in the last-stage quantizer, for oversampling ratios from 8 to 24: (a) 2-1^2 \( \Sigma\Delta \)M, (b) 2-1^3 \( \Sigma\Delta \)M. (\( A_{DC} = 2500 \), \( \sigma_C = 0.12\% \), and DAC INL = 0.4\%FS).
\(B\) tends to saturate due to the presence of leakages. In fact, when increasing the last quantizer resolution in 1 bit generates less than 1-bit increase in the overall modulator resolution, the dual-quantization architecture starts losing efficiency and may become unsuitable for the specifications and technology considered.

Nevertheless, depending on the signal bandwidth, the reduction in oversampling ratio that can be achieved by resorting to multi-bit quantization may define the border between feasible and unfeasible implementations. For instance, let us consider the 4th-order cascade (2-1^2 \(\Sigma\Delta\)M) in order to obtain 14-bit effective resolution. According to Fig. A.6a, its single-bit version would require \(OSR = 24\), whereas a 3-bit version with \(OSR = 16\) is also feasible. For a signal bandwidth of 2.2MHz, the oversampling ratios mean 105.6-MHz and 70.4-MHz clock rate, respectively. Apart from an eased testing, certain power saving can be expected by using the multi-bit modulator.
APPENDIX B

Power Estimator for Cascade $\Sigma\Delta$ Modulators

In this Appendix we present an analytical procedure to estimate the power consumption of single-bit and multi-bit cascades $\Sigma\Delta$Ms based on the expandible $L$th-order $2^{-1}L-2$ topology proposed in Appendix A.

Both architecture and technological features are contemplated in the underlying expressions, together with simplifying assumptions inspired in practical design solutions.

B.1 Dominant Error Mechanisms

Let us start assuming that, in whatever practical design of a high-frequency $\Sigma\Delta$ modulator, the dominant sources of in-band error power are quantization error, white circuit noise, and incomplete settling error. The latter is specially important for telecom converters, in which a sampling frequency at the edge of the CMOS feasibility will have to be used.

Under these initial assumptions, the dynamic range ($DR$) of the $\Sigma\Delta$ modulator can be roughly expressed as follows

$$DR = 3 \cdot 2^{2\text{ENOB}-1} \approx \frac{V_{\text{ref}}^2}{P_Q + P_{\text{CN}} + P_{\text{st}}}$$

where $V_{\text{ref}}$ is the reference voltage that determines the modulator full scale ($\Delta = 2V_{\text{ref}}$) and $P_Q$, $P_{\text{CN}}$, and $P_{\text{st}}$ are the in-band powers of quantization error, white circuit noise or thermal noise, and settling error, respectively.

The selection of the reference voltage impacts $P_Q$ and, although more indirectly, also $P_{\text{CN}}$ and $P_{\text{st}}$. Moreover, $V_{\text{ref}}$ is obviously constrained by the supply voltage, because it imposes a given output swing requirement in integrators, which must be feasible in the intended technology. In conclusion, the selection of $V_{\text{ref}}$ is closely related to the amplifier topology and its capability to trade DC gain, speed, and output swing [Raza00] [Malo01].
practice, an upper bound for a feasible selection of $V_{\text{ref}}$ is given by \(^\dagger\)

\[
V_{\text{ref}} = V_{\text{supply}} - n_{\text{ob}} V_{\text{sat}}
\]  

where $V_{\text{sat}}$ is the saturation voltage of the amplifier output devices and $n_{\text{ob}}$ is the number of transistors in the output branch, which again depends on the specific amplifier topology. If a single-stage amplifier is used, cascode devices will be required to achieve enough DC gain, so that $n_{\text{ob}} \geq 4$. This common choice is not adequate in low-voltage implementations, where an excessive value of $V_{\text{sat}}$ will result in a very small value for $V_{\text{ref}}$.

Among the alternatives, two-stage amplifiers offer the possibility to still yield a large open-loop DC gain, while their output branches can contain only two transistors ($n_{\text{ob}} = 2$). This allows to increase the value of the reference voltage and to set the modulator full scale to a useful level.

Next, for the sake of simplicity, we will assume for the time being that settling error can be controlled by design so that $P_{st} \ll P_Q$, $P_{CN}$; i.e., eq(B.1) simplifies to

\[
DR \approx \frac{V_{\text{ref}}^2/2}{P_Q + P_{CN}}
\]  

With respect to $P_Q$, it is formed by three main error mechanisms:

- Last-stage quantization error,
- Last-stage DAC non-linearity (only if multi-bit quantization is used), and
- Non-cancelled portion of the low-order quantization errors caused by integrator leakage and capacitor mismatch.

A close expression including the former non-idealities can be obtained for the expandible $2^{-1L^{-2}}$ cascade $\Sigma\Delta$M by adding up equations (A.4) and (A.5), what results in

\[
P_Q = 4\sigma_Q^2 \cdot \frac{\pi^{2L}}{(2L + 1)OSR^{2L + 1}} + 4\sigma_D^2 \cdot \frac{\pi^{2L - 1}}{(2L - 1)OSR^{2L - 1}} + \frac{(2V_{\text{ref}})^2}{12} \cdot \left( \frac{25}{16A_{\text{DC}}} \cdot \frac{\pi^2}{3OSR^3} + \frac{36\sigma_C^2}{5OSR^5} \right)
\]  

with

\[
\sigma_Q^2 = \frac{1}{12} \cdot \left( \frac{2V_{\text{ref}}}{2\delta - 1} \right)^2 \quad \sigma_D^2 = \frac{1}{2} \cdot (2V_{\text{ref}})^2 \cdot \left( \frac{\text{INL}}{100} \right)^2
\]  

1. A fully-differential modulator employing symmetrical references $\pm V_{\text{ref}}$ is assumed.
where $\sigma_1^2$ is the power associated to the last-stage quantization error ($B$ stands for the resolution of the multi-bit quantizer), $\sigma_2^2$ is the error power associated to the DAC, with $\text{INL}$ being the DAC integral non-linearity in $\%$FS, $A_{DC}$ stands for the 1st-stage amplifier DC gain, and $\sigma_C$ is the capacitor standard deviation.

Concerning $P_{CN}$, it is usually dominated by the white noise injected by the switches and the front-end amplifier, whose $\text{PSD}$ is folded-back over the baseband by undersampling. A conservative expression for the in-band power of white noise can be derived (see Section 2.4.2)

$$P_{CN} = P_{kT/C} + P_{op} \approx 2 \cdot \frac{2kT}{C_S} \cdot \frac{1}{\text{OSR}} + \frac{4kT}{3C_S} \cdot \frac{1}{\text{OSR}} = \frac{16kT}{3C_S} \cdot \frac{1}{\text{OSR}} \quad \text{(B.6)}$$

where $C_S$ is the value of the sampling capacitor.

### B.2 Estimation of Power Consumption

Equations (B.3) to (B.6) show that the dynamic range of a cascade $\Sigma\Delta M$ can be roughly expressed as a function of the following design parameters: $L$, $\text{OSR}$, $C_S$, $A_{DC}$, and $\sigma_C$, to which we have to add $B$ and $\text{INL}$ if the last-stage quantizer is multi-bit. So, for given values of $A_{DC}$, $\sigma_C$, and $\text{INL}$, the minimum value of the capacitor $C_S$ required to obtain a given $\text{DR}$ can be obtained as a function of $L$, $\text{OSR}$, and $B$. Once $C_S$ is known, the equivalent load for the amplifier in the integrator can be estimated as

$$C_{eq} \cong C_S + C_p + C_L \left( 1 + \frac{C_S + C_p}{C_I} \right) \quad \text{(B.7)}$$

where $C_I$, the integrator feedback capacitance, is related to $C_S$ through the integrator weight ($C_I = C_S/g_i$) whereas $C_p$ and $C_L$ stand for the integrator summing node and output node parasitics, respectively. Estimating the latter two capacitances is a difficult task because of their extreme dependence on the actual amplifier design.

Usually, the main contribution to $C_p$ is the amplifier input parasitic. In a fully-differential topology, it is formed by the input transistor gate-to-source capacitance $C_{gs}$ (both channel and overlap contributions) and its overlap gate-to-drain capacitance $C_{gvd}$ amplified by Miller effect [Raza00]. Neglecting $C_{gb}$,

$$C_p \cong C_{ch} + C_{ov} + C_{ov}(1 + A_{DC}) = \frac{2}{3} C_{ox} W_{in} \cdot L_{in} + C_{ox} W_{in} \Delta L_{in} (A_{DC} + 2) \quad \text{(B.8)}$$

where $C_{ox}$ is the gate oxide capacitance density and $\Delta L_{in}$ stands for the lateral
diffusion of drain/source regions below the gate, both technology-dependent parameters. Apart from the input transistor dimensions \((W_{in}, L_{in})\), the other unknown variable in eq.(B.8) is its input-to-output gain \(A_{DC1}\). This is equal to the complete amplifier gain for single-stage amplifiers or to the 1st-stage gain if multi-stage topologies are used. It can even be around unity if cascode devices are used, such as in telescopic or folded-cascode amplifiers [Raza00] [Malo01]. Now, making use of the well-known (as much as inadequate) square-low expression for the input transistor drain current

\[
P_{o} = \frac{2L_{in}I_{D,dr}}{\Delta V_{OVD}} \left[ \frac{2}{3}L_{in} + \frac{1}{A_{DC1}} + 2 \right]
\]

where \(V_{OVD} = V_{GS} - V_{T}\) is the input transistor overdrive voltage.

The other unknown capacitance in eq.(B.7), \(C_L\), has two main contributions: the first one is due to the bottom parasitic of the integration capacitor \(C_I\) and the second one is due to the amplifier itself. The former contribution can significantly vary depending on the type of capacitors. With modern MiM structures it turns out to be very small, ranging from less than 1% to 5% of \(C_I\). Because of this, \(C_L\) tends to be dominated by the amplifier output parasitic load, which strongly depends on the actual output devices and, overall, on the amplifier topology. Even the supply voltage, via output swing and DC-gain requirements, makes an impact on the transistor sizes and hence on \(C_L\). For a given amplifier schematic, the latter influence makes \(C_L\) slightly increase under technology scaling and shrinking supply voltages, because wider output devices are required to accommodate similar output swings. All things considered, a reliable estimation of this capacitance prior to the sizing of the amplifier is not possible. Based on previous design experiences, we will assume a constant value equal to 2.5pF.

Returning to the settling error power, \(P_{st}\), an accurate estimation would involve the following calculations. For example, just for a single-pole amplifier model, complicate expressions are derived [Mede99a] if a non-linear (slew-rate limited) settling is considered. Further complexity arises from considering both sampling and integration incomplete charge-transference and the contribution of the non-zero switch on-resistance (see Section 2.3). Hence, the treatment will be simplified assuming that the slew rate of the amplifier is large enough and the switch on-resistance small enough to neglect their impact on the integrator transient response, so that the settling is linear with time constant equal to \(C_{eq}/g_{m}\). This being the case, it takes a number \(\ln(2^{ENOB})\) of time constants to settle within \(ENOB\) resolution; i.e., the following relationship should be fulfilled

\[
\ln[2^{(ENOB + 1)}] C_{eq}/g_{m} \leq T_s/2
\]
B.2 Estimation of Power Consumption

where $T_s$ is the sampling period. Note that an extra bit has been added in order to make room for the inaccuracy of this simplified model. The above expression can be used to estimate the minimum value of the transconductance parameter

$$g_m = 2\ln[2^{(ENOB + 1)}]C_{eq}f_s \quad (B.11)$$

where $f_s = 1/T_s$ is the sampling frequency. This is the transconductance required for a single-stage amplifier with equivalent output load $C_{eq}$. For multi-stage amplifiers, the previous relationship must be carefully tackled because both parameters, total transconductance and equivalent output load, lose control of the amplifier dynamics. However, provided that the main pole of the amplifier is set by the input stage and an eventual inter-stage compensation capacitor, eq(B.11) can still be used to determine the input stage transconductance, that is related to the input transistor current as follows

$$g_m = \frac{2I_{D, in}}{V_{OVD}} \quad (B.12)$$

Equations (B.7), (B.9), (B.11), and (B.12) can be handled in an iterative way to determine the current required through the input transistors of the amplifier, whose actual topology sets the power consumption. Whenever possible, a single-stage amplifier should be used because of its better performance/power figure. However, as discussed previously, as technologies scale down and supply voltages shrink, two-stage amplifiers are gaining ground. Moreover, in practice two gain stages are not enough to achieve the overall gain requirement, so that the first one often includes cascode devices in a telescopic-cascode configuration. Let us consider this topology as an archetype in modern deep-submicron technologies. The current through the first stage has been already estimated as $I_B$. Assuming, for the sake of simplicity, a fixed ratio $\eta_{io}$ between the currents flowing through the input and output branches, the total current through the amplifier can be estimated as

$$I_B \geq 2I_{D, in} + 2\eta_{io}I_{D, in} + I_{D, in} = [2(1 + \eta_{io}) + 1]I_{D, in} \quad (B.13)$$

where an extra $I_{D, in}$ has been added to account for the biasing stage of the amplifier.

The power dissipation of the first amplifier can be estimated with eq(B.13). That of the remaining amplifiers in the cascaded stages can be decreased, following the scaling rule commonly applied to amplifier requirements in $\Sigma\Delta$ modulators. This power reduction may come from either a relaxed set of specifications or the subsequent simplification of the amplifier topology. Sometimes, even when a two-stage amplifier may be required for the first integrator, it is possible to use a single-stage topology for the rest of integrators. So, we can write
with $\chi_i$ being the ratio of the current absorption of the $i$-th amplifier to the first one. From this, the static power dissipated in the amplifiers is:

$$P_{\text{op, sta}} = I_B V_{\text{supply}} \left( 1 + \sum_{i=2}^{L} \chi_i \right)$$  \hspace{1cm} (B.15)$$

Besides this static consumption, which usually accounts for around 80% of the total power, there are other contributing blocks, namely:

- $L - 1$ latched comparators used as single-bit quantizers and those in the last-stage multi-bit quantizer, usually implemented by a flash ADC; i.e., $(2^B - 1)$ more latches. This consumption must include the static power dissipated in a convenient pre-amplifying stage.

- Last-stage multi-bit DAC (if $B > 1$). The relaxed requirements for this block allows us to implemented it with a resistor ladder. Its main design considerations are resistor matching and linearity (both causing $\text{INL}$) and the current it must drive, which must be large enough to provide a good settling. The current requirement scales with the sampling frequency and the capacitive load involved. The latter can be considered almost constant, because the last-stage capacitors should be set to the minimum required to achieve certain level of matching (thermal noise playing a secondary role). So, we can empirically write

$$P_{\text{DAC}} \approx V_{\text{supply}} I_{\text{DAC}}^* \frac{f_s}{f_s^*}$$  \hspace{1cm} (B.16)$$

where $I_{\text{DAC}}^*$ is the current through the DAC required for operating at a certain frequency of reference, $f_s^*$.

- Dynamic power in SC stages. The dynamic power dissipated to switch a capacitance $C_i$ between the reference voltages at a frequency $f_s$ can be estimated as $C_i f_s V_{\text{ref}}^2$, which tends to increase in high-speed high-resolution converters. Its actual value depends on the integrator weights used. In our case, the following expression provides a good estimate

$$P_{SC} = 2[5C_{u_1} + 4(L - 1)C_{u_2}]f_s V_{\text{ref}}^2$$  \hspace{1cm} (B.17)$$

where the factor 2 comes from the differential implementation; $C_{u_1}$ is the unit capacitor used in the first integrator, whereas $C_{u_2}$ is the one used in the rest of integrators, usually smaller than $C_{u_1}$.
• Small digital blocks: flip-flops, gates, cancellation logic, etc. Apart from being small, they do not make any difference for the architectures considered and will be neglected here. Of course, this does not apply to the decimation filter, whose power consumption is comparable to that of the \( \Sigma \Delta \) modulator. Moreover, since the order of the digital filter must equal \( L + 1 \), high-order \( \Sigma \Delta \)Ms require more complex filters than low-order ones. However, an increase of the modulator order entails a decrease of the oversampling ratio and the filter can be operated at a lower frequency, dissipating less power. To our purpose, we can consider an essentially constant power consumption in the digital filter.

By adding up all the contributions, the power dissipation of the cascade \( \Sigma \Delta \) modulator can be estimated as:

\[
\text{Power} \approx P_{op, \text{sta}} + P_{DAC} + [(L - 2) + (2^B - 1)]P_{comp} + P_{SC} \quad (B.18)
\]
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