Index

1-T cell
- 1-T-based cells, 85–87
  - data-line arrangement, 85–87, see also folded-data-line 1-T cell
  - data-line precharging schemes, 87
  - gain cells, 82–85
  - and related cells, 80–81
- 2-T cell, design of, 110–112
- 3-T cell, 80, 82
  - gain cells, 82
- 4-T cell, 80, 82
  - data-retention characteristics, 121
  - gain cells, 82
- 6-T SRAM cell
  - 1-T DRAM cell versus, 139–147
  - leakage currents in, 122–124
  - voltage margin of, 124–129
    - improvements, 130–138, see also separate entry
  - read and write voltage margin, 125
  - signal charge, 126–129
- 6-T SRAM cell, voltage margin of, 124–129
  - improvements, 130–138
  - cell layout, lithographically symmetric, 130–131, see also separate entry
  - fully-depleted SOI cells, 135–138
  - power-supply controlled cells, 131–135, see also separate entry

bipolar transistors, common-centroid layout of, 225
body-bias generator for nMOST, 191
boosted sense-ground (BSG), 91
buried-oxide (BOX) double-gate FD-SOI MOST, 112, 136
nanometer era, role in, 193–195
burn-in test, design for, 219–224
burn-in voltage generator, 205
  - principle, 209–211

cell array layout, 84
cell layout, lithographically symmetric, 130–131
conventional SRAM cell versus, 131
  - cell operations, 139–140
  - flip-flop circuits, see separate entry
  - memory cell size, 146–147
  - soft-error immunity, 145–146
channel length modulation, 6
charge pump, 23–24
  - high efficient two-phase, 305
circle-gate sense amplifier, 101
circuit simulation, models used in, 126
closed-loop gain, 247
CMOS analog circuit
  - basic circuit, 29–32
    - common-source amplifier, 30–31
    - current mirror circuit, 29–30
    - differential amplifier, 31–32
  - basics, 24–32
digital circuits, comparison, 24–26
equivalent circuits, 26–29, see also separate entry
CMOS digital circuits
  - analog circuit versus, 24–26
  - basics, 19–24
  - charge pump, 23–24
  - CMOS inverter, 20
  - cross-coupled CMOS sense amplifier, 21–23
  - level shifter, 23

alpha-particle induced soft error, 56

bandgap reference (BGR) circuit, 209–218
  - circuit design, 211–213
  - low supply voltage, bandgap $V_{REF}$
    - generators for, 215–218
    - operating principle, 209
    - parasitic npn transistor, 211
    - parasitic pnp transistor, 213
    - variation of reference voltage, 214–215
  - bandgap $V_{REF}$ generator, 209–218
    - for low supply voltage, 215–218
Index

NOR and NAND gates, 21
ring oscillator, 24–25
CMOS inverter, 20
common-mode noise, 85, 95
components, 97–98
noise reduction, 102–104
compensation capacitor, 262
complementary-MOS (CMOS), see CMOS
cosmic ray
cross-coupled CMOS sense amplifier, 21–23
nMOS sense amplifier, operations, 22
pMOS sense amplifier, operations, 22
current-mirror circuit, layout of, 226
cutoff region, 3
data-line capacitance, 81
data-line contacts (DCT), 105
data-line precharging scheme
types, 87
data-line shielding circuits, 110
data-retention time
definition, 12
derepletion nMOST (DnMOST), 2
transfer characteristics, 3
derepletion pMOST (DpMOST), 2
transfer characteristics, 3
derepletion-mode output transistor, 237
destructive read-out (DRO) memory
cell, 37, 84
development trends
DRAM cells, 80–85
SRAM cells, 120–122
device simulation, models used in, 126
Dickson type converter
charge pump circuits, 310
switched capacitor type converter versus, 286, 309–313
charge recycling multiplier, 311–313
influences of parasitic capacitances, 309–311
differential amplifier
offset voltage of, 214
small-signal equivalent circuit, 250
PSRR analysis, 264
differential-mode noise, 85, 95
components, 96–97
noise reduction, 101–102
dominant pole compensation
circuit diagram, 254
small-signal equivalent circuit, 254
double-gate fully-depleted SOI cells
DRAM cells, design of, 112–115
SRAM cells, 137–138
double-polysilicon stacked gate cell, 50
drain conductance, 28
RAM cells
1-T cell, 80–81, see also separate entry
2-T cell, design of, 110–112
data-line precharging scheme, 87
development trends, 80–85
double-gate fully-depleted SOI cells, design of, 112–115
e-DRAM vs conventional DRAM, 81
folded-data-line 1-T cell, design of, see separate entry
gain cells, 82–85, see also separate entry
minimum \( V_{DD} \), of, 144
open-data-line 1-T cell, design of, see separate entry
operation of, 93
ultra-low voltage nano-scale, 79–115
DRAM peripheral circuits
256-Mb DRAMs, gate-source (VGS)
self-reverse biasing in, 171
architecture, 65
basics, 37–42
DRAM array, 38
leakage reduction, 170–176
256-Mb SDRAM, 172
active-current reduction for a 16-Gb
DRAM, 171–175
cell relevant circuits of 0.6-V 16-Mb
e-DRAM, 176
row circuits of 0.6-V 16-Mb
e-DRAM, 177
sense-amp driver of 0.6-V 16-Mb
e-DRAM, 177
sleep-mode current reduction in 90-nm
16-Mb e-DRAM, 175–176
standby-current reductions in 256-Mb
DRAMs, 170–171
read operation, 38–40
refresh operation, 41–42
write operation, 40
Dual \( V_{DD} \) processor, 146
Dynamic Random Access Memories, see DRAM cells
enhancement nMOST (E-nMOST), 2
circuit expressions, 3
E-nMOST capacitor, 8–9
transfer characteristics, 3
voltage relationships, 3
enhancement pMOST (E-pMOST), 2
circuit expressions, 3
transfer characteristics, 3
voltage relationships, 3
equivalent circuits, 26–29
large-signal equivalent circuit, 26–27
voltage down-converter, 240
small-signal equivalent circuit, 27–29, see also separate entry
erase operation, NOR cell, 51
error checking and correction (ECC) circuit, 57, 59–60, 189–190
feedback type voltage doubler, 291
flash memories, 45–56
cross-section, 46
flash memory cell, 46
flash memory cells, basic operation of, 45–50
NAND cell, 53–56
NOR cell, 50–53
read operation, 47
flip-flop circuits, 140–143
symmetric layouts, 190
variations in Vt mismatch of, 186–189
voltage margin, 141–142
Vt-relevant parameters, variations in, 142–143
floating-body-transistor cell (FBC), 82–84
principle, 83
folded-data-line 1-T cell, design of, 87–104
effective signal voltage and the gate-over-drive of SAs, 98–101
lowest necessary threshold voltage and word line voltage, 87–91
minimum $V_{DD}$, 91–92, 104
noise reduction, 101–104
noise sources, 93–98
signal charge and signal voltage, 92–93
Fowler-Nordheim (FN) tunneling mechanism, 47–49
gain cells, 82–85
1-T cell, 82–85
3-T cell, 82
4-T cell, 82
high-voltage tolerant circuits, 327–337
concepts, 328–330
gate-applied high-voltage tolerant circuit, 329
hot-carrier tolerant circuit, 329
hot-carrier injection mechanism, 328
i/o circuits, applications to, 333–337
input buffers, 336–337
output buffers, 333–336
internal circuit, applications to, 330–333
level shifter, 330–332
voltage doubler, 332–333
necessity, 327–328
hot-carrier injection mechanism, 18
hot-electron injection (HEI) mechanism, 47–48
hybrid pumping $V_{BB}$ generator, 300
input buffers, high-voltage tolerant, 336–337
internal supply voltages, 70–73
dynamic control of, 72–73
static control of, 70–71
large-signal equivalent circuit, 26–27
voltage down-converter, 240
layout
bipolar transistors, common-centroid layout of, 225
current-mirror circuit, 226
on-chip voltage down converter, 227
paired MOSTs layout, 224
common-centroid layout of, 225
resistors, 226
leakage current, 14–19, see also leakage reduction circuits
in 6-T SRAM Cell, 122–124
components, 134
in DRAM cells, 87–88
gate-tunneling current, 16–17
characteristics, 16
conventional word driver, 17
gate-tunneling-current-suppressed word driver, 17
pn-junction current, 18–19
forward pn-junction current, 19
substrate current, 17–18
hot-carrier injection mechanism, 18
subthreshold current, 14–16
types, 14
leakage reduction circuits, 154–158
applications to RAMs, 166–179
DRAM peripheral circuits, applications to, 170–176, see also DRAM
peripheral circuits
peripheral circuits features, 168–170, see also peripheral circuits of RAMs
SRAM peripheral circuits, applications to, 176–179, see also SRAM peripheral circuits
basic concepts, 154–157
gate-source offset driving, 156–157
gate-source self-reverse biasing, 155–156
offset source driving, 157
substrate (well) driving, 157
reduction circuits versus, 157–158
level shifter, 23, 74, 330–332
high-voltage tolerant circuits, 330–332
logic circuits
RAMs, 151–179, see also RAMs
LSI design
CMOS analog circuit, 24–32, see also separate entry
CMOS digital circuits, 19–24 see also separate entry
DRAMs basics, 37–42
DRAM array, 38
read operation, 38–40
redundancy techniques, 57–59
refresh operation, 41–42
write operation, 40
flash memories, 45–56
cross-section, 46
flash memory cells, basic operation of, 45–50
NAND cell, 53–56
NOR cell, 50–53
read operation, 47
future memories, power management for, 68–73
internal supply voltages, dynamic control of, 72–73
internal supply voltages, static control of, 70–71
introduction, 1–74
leakage currents, 14–19, see also separate entry
LSI devices, basics of, 1–14
MOST characteristics, 1–9
resistors, 13–14
memory LSI, see under separate entry
on-chip voltage converters, 73–74
power supply schemes, 63–66
dual power supply, 64
single power supply, 64
power supply voltages, trends in, 66–68
scaling laws, 60–63
combined scaling, 63
constant electric-field scaling, 60–62
constant operation-voltage scaling, 62–63
scaling approaches, 62
soft error, 56–57
SRAMs basics, 42–45
read operation, 42–44
SRAM array, 43
write operation, 44–45
memory cells, 35–37
DRAM cell, 36
memory-cell array, 36
NAND flash memory cell, 36
SRAM cell, 36
memory chip architecture, 34–35
memory LSI
basics of, 32–37
destructive read-out (DRO) memories, 37
memory cells, 35–37, see also separate entry
memory chip architectures, 34–35
non-destructive read-out (NDRO) memories, 37
VLSI memories
memory capacity, trends in, 33
memory-cell size, trends in, 33
metal-insulator-metal (MIM) stacked capacitor, 81
Metal-Oxide-Semiconductor Transistor (MOST)
bulk MOSTs, 9–11
double-well structures, 9
nMOST structures, 11
parasitic bipolar transistors, 10
triple-well structures, 9
characteristics, 1–9
deployment nMOST (DnMOST), see separate entry
enhancement nMOST (E-nMOST), see separate entry
enhancement pMOST (E-pMOST), see separate entry
gate-source reverse biasing schemes, see separate entry
leakage current, 152
leakage reduction, basic concepts for, 152–154
leakage reduction circuits, see separate entry
leakage reduction efficiency, 154
n-channel MOST (nMOST), see separate entry
paired MOSTs layout, 224
common-centroid layout of, 225
small-size effects, 7
narrow-channel effect, 7
short-channel effect, 7
SOI MOSTs, see individual entry
standby subthreshold current, 69
Miller compensation, 260–261
circuit diagram, 260
gain and phase characteristics, 260
small-signal equivalent circuit, 260, 265
multi-stage amplifier, 243
gain and phase characteristics, 245
NAND gate, 21
  dynamic NAND, 21
NAND architecture, 54
  read operation, 55
static NAND, 21
nanometer era, variability issue in, 183–195
  leakage variations, 184–185
  1-Mb array current vs. Vt of cross-coupled MOSTs, 185
reductions, solutions for, 189–193
  controls of internal supply voltages, 190–192
  fully-depleted SOI, 193–195
  raised power supply voltage, 192–193
  redundancy and ECC, 189–190
  symmetric layouts for flip-flop circuits, 190
  speed variations of logic circuits, 185–186
  speed variations of an inverter, 186
  variations in Vt mismatch of flip-flop circuits, 186–189
CMOS, standard deviation of Vt-mismatch for, 187
  maximum Vt-mismatch ratio, 188
Vt variation, 183–184
  standard deviations, 184
n-channel MOST (nMOST) cross-section, 1–9
negative voltage generators
  Dickson-type voltage multiplier, 306–307
  for low-voltage operation, 307
  equivalent circuit, 294
level monitor, 318
  using resistor divider, 318
operating waveform, 294
simplified circuit, 294
switched-capacitor (SC)-type voltage multipliers, 307–309
  using inductor, 313–316
  circuit diagram, 316
  timing diagram, 316
with capacitor, 293–295
  applications to memories, 297–301
negative word-line (NWL), 91
  voltage scheme, 52–53
noise reduction
  common mode, 102–104
  differential mode, 101–102
  folded-data-line 1-T cell, 101–104
  open-data-line 1-T cell, 107–110
noise sources, 93–98
  common-mode noise, see separate entry
  differential-mode noise, see separate entry
non-destructive read-out (NDRO) memories, 37, 139–140
non-saturated region, 4
NOR gate, 21
  dynamic NOR, 21
  erase operation, 51
  read operation, 51
static NOR, 21
  write operation, 51
offset gate driving
  application to power switch, 156
  application to RAM cells, 156
  principle, 156
offset voltage
  of differential amplifier, 214
  output-voltage error, relationship with, 216
on-chip substrate bias, 130
on-chip voltage converters, 73–74
open-data-line 1-T cell, design of, 104–110
  data-line shielding circuits, 110
noise reduction, concepts for, 107–110
noise-generation mechanism, 105–107
  optical proximity correction (OPC), 130
  output buffers, high-voltage tolerant, 333–336
  output-voltage error
    offset voltage, relationship with, 216
parasitic bipolar transistors
parasitic npn transistor
  bandgap reference circuit using, 211, 213
cross sections of, 210
parasitic pnp transistor
  bandgap reference circuit using, 213
cross sections of, 210
partially-depleted silicon-on-insulator (PD-SOI), 83
peripheral circuits of RAMs, 168–170
  features, 168–170
  input-predictable circuits, 168–169
  internal power-supply voltages, 170
  multiple iterative circuit block, 168
  robust Circuit, 170
  slow RAM cycle, 169–170
pMOST
  cross-coupled VBB generator, 300
  transfer switch, 293
pole-zero compensation
  circuit diagram, 256
  gain and phase characteristics, 256
  phase margin vs. load parameters, 259
  small-signal equivalent circuit, 256
power supply rejection ratio (PSRR), 262–265
  small-signal equivalent circuit, 263
Index

power supply voltage
  microcontrollers, 67
  RAMs, 67
power-supply controlled cells, 131–135
dynamic control of cell-power line, 135
offset source driving cell, 133–135
raised power supply cell, 131–133
programming disturbs, 52

RAMs
  leakage reduction circuits, see separate entry
  leakage sources, 167–168
  array driver blocks, 168
  control logic block and others, 168
  row and column decoder blocks, 168
  sense amplifier block, 168
  logic circuits, leakage reduction for, 151–179
  minimum V<sub>DD</sub> of, 143–146
  cell and sense amplifier, 143–145
  peripheral logic circuits, 145–146
  peripheral circuits features, 168–170, see also peripheral circuits of RAMs
  power supply voltages, trends in, 67
  principle of on-chip ECC for, 59
  RAM chip, architecture of, 167
  sleep mode, 169
read data line, 80
read operation
  DRAM, 38–40
  NAND gate, 55
  NOR cell, 51
  SRAM, 42–44
read word line, 80
reference voltage converter/trimming circuit, 218–224
  basic design, 218–219
  burn-in test, design for, 219–224
  burn-in voltage condition, 219–220
  burn-in voltage generation, 220–224
  circuit and its characteristics, 222–223
  on-chip voltage down converter, using, 219
  uniform acceleration throughout chip, 220
  voltage variation before and after trimming, 224
reference voltage generators, see under voltage generators, reference
refresh time, 82
dynamic, 88
resistors, layout of, 226
ring oscillator, 24–25
saturated region, 4–5
scaling laws, 60–63
  combined scaling, 63
  constant electric-field scaling, 60–62
  constant operation-voltage scaling, 62–63
  scaling approaches, 62
self-aligned contact (SAC), 80, 83
self-reverse biasing circuits
  operating waveforms, 155
  principle, 155
  source driving, 157
  operating waveforms, 157
series regulator, 233–269
  AC characteristics and phase compensation, 243–261
  compensation, 253–262
  phase compensation methods versus, 253
  phase margin, 248–253
  simulation method, 251
  stable conditions, 243–248
  applications, 267–269
  circuit diagram, 233
  DC characteristics, 234–239
  error amplifier, 232–234
  low-power design, 265–267
  power supply rejection ratio (PSRR), 262–265
  transient characteristics, 239–243
  signal-to-noise-ratio (S/N), 79, 119
  single-stage amplifier
  gain and phase characteristics, 244
  small cell capacitance, 81
  small-signal equivalent circuit
  differential amplifier, 250
  dominant pole compensation, 254
  inverter circuit, 29
  Miller compensation, 260
  PSRR analysis, 263
  small-size effects, 7
    in a MOST
      narrow-channel effect, 7
      short-channel effect, 7
  soft error, 56–57
    alpha-particle induced, 56
    soft-error rate (SER), 147
SOI (Silicon-On-Insulator) MOST
  data-retention characteristics, 12
  FD-SOI
    nMOST structures, 11
  PD-SOI
    nMOST structures, 11
  source-follower mode, 5–6
SRAM cells
  6-T SRAM Cell, leakage currents in, 122–124
basics, 42–45
  read operation, 42–44
  write operation, 44–45
development trends, 120–122
minimum $V_{DD}$ of, 144
power controls of, 132
read failure of, 124
signal charge, 126–129
thin-film-transistor (TFT), using, 121
ultra-low voltage nano-scale, 119–147
voltage margin of the 6-T SRAM cell, 124–129
SRAM peripheral circuits
leakage reduction, 176–179
multi-bank architecture, 178–179
startup circuit, design of, 212
static noise margin (SNM), 130–131
Static Random Access Memories, see SRAMs
substrate-source voltage ($V_{RS}$) reverse biasing circuits, 157
offset source driving, 157
substrate (well) driving, 157
application to power switch, 157
operating waveforms, 157
subthreshold current
reduction circuits, 70
standby subthreshold current, 69
switched capacitor type converter
charge pump circuits, 310
Dickson type converter versus, 286, 309–313
charge recycling multiplier, 311–313
influences of parasitic capacitances, 309–311
voltage multiplier
  equivalent circuit, 308
  simplified circuit, 308
switched-capacitor regulator, 272–276
equivalent circuit, 273, 275
operating waveforms, 274
switched-capacitor voltage halving circuit, 273
switching regulator, 269–272
divided-switch technique, 272
operating waveforms, 270
switching-noise reducing scheme, 271
thin-film-transistor (TFT), 121

Ultra-low voltage nano-scale cells
  DRAM cells, 79–115, see also separate entry
  SRAM cells, 119–147, see also separate entry
variability issue in nanometer era
  voltage doubler, 237, 288–293, 332–333
circuit diagram, 288
equivalent circuit, 289
external voltage vs. boosting ratio, 292
feedback type 291
feedback type, 291
high-voltage tolerant circuits, 332–333
operating mode, 289
operating waveform, 288
pMOST transfer switch, 293
transfer switch, 292
voltage down-converters, 231–281
conversion efficiency versus, 232
half-$V_{DD}$ generator, 277–279
large-signal equivalent circuit, 240
nMOST-output circuit, 234
current driving capability, 236
open-loop small-signal equivalent circuit, 249
parallel connection, 266
phase margin, 248–253
loop gain, relationship with, 279–281
simulation method, 251
pMOST-output circuit, 235
current driving capability, 236–237
series regulator, 233–269, see also separate entry
switched-capacitor regulator, 272–276, see also separate entry
switching regulator, 269–272, see also separate entry
types, 231
voltage down-converters versus, 232
voltage follower
  using negative feedback, 245
voltage generators, reference, 198–227
  application of $\Delta V$, $V_{REF}$ generator, 206–209
  bandgap $V_{REF}$ generator, see under separate entry
comparison of, 200
reference voltage converter/trimming circuit, see under separate entry
threshold voltage, based on
  nMOST, 200
  with improved temperature coefficient, 201–202
threshold-voltage difference, based on between enhancement and depletion
  MOSTs, 203
  between pMOSTs, 204–206
temperature dependency, 208
$V_{REF}$ generator, layout design of, 224–227
$V_t$-difference ($\Delta V_t$) $V_{REF}$ generator, 203–209
  basic $\Delta V_t$ $V_{REF}$ generator, 203–206
  $V_t$-referenced $V_{REF}$ generator, 200–203
voltage margins, types of, 125
voltage up-converters, 73
  basic voltage converters with capacitor, 288–301
  applications to memories, 296–297
  voltage doubler, see separate entry
Dickson-type voltage multiplier, 301–306
  for low-voltage operation, 303–305
  efficiency analysis, 318–324
  Dickson type charge pump circuit, 318–321
switched-capacitor-type charge pump circuit, 321–324
  level monitor, 317–318
  using resistor divider, 317
switched-capacitor (SC)-type voltage multipliers, 307–309
  fractional voltage up-converters, 308–309
  with an inductor, 313–316
voltage-down converter (VDC), 64–65
WL pumping mechanism, 84
  word boosting, 90–91
  boosted sense-ground (BSG), 91
  negative word-line (NWL), 91
word driver
  conventional, 17
  gate-tunneling-current-suppressed word driver, 17
word-line voltage, 87–91
write data line, 80
write operation
  DRAM, 38–40
  NOR cell, 51
  SRAM, 44–45
write word line, 80