<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
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<tbody>
<tr>
<td>API</td>
<td>Application Programming Interface</td>
</tr>
<tr>
<td>ASIP</td>
<td>Application Specific Processor</td>
</tr>
<tr>
<td>ATPG</td>
<td>Automatic Test Pattern Generation</td>
</tr>
<tr>
<td>BCA</td>
<td>Bus Cycle Accurate</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary Metal Oxide Semiconductor</td>
</tr>
<tr>
<td>CODEC</td>
<td>Coder/Decoder</td>
</tr>
<tr>
<td>CPU</td>
<td>Central Processing Unit</td>
</tr>
<tr>
<td>DCT</td>
<td>Discrete Cosine Transformation</td>
</tr>
<tr>
<td>DMA</td>
<td>Direct Memory Access</td>
</tr>
<tr>
<td>DOM</td>
<td>Document Object Model</td>
</tr>
<tr>
<td>DSP</td>
<td>Digital signal processing</td>
</tr>
<tr>
<td>DUT</td>
<td>Design Under Test</td>
</tr>
<tr>
<td>EDA</td>
<td>Electronic Design Automation</td>
</tr>
<tr>
<td>eDRAM</td>
<td>Embedded Dynamic Random Access Memory</td>
</tr>
<tr>
<td>FIFO</td>
<td>First-In-First-Out</td>
</tr>
<tr>
<td>FPGA</td>
<td>Field Programmable Gate Array</td>
</tr>
<tr>
<td>FSM</td>
<td>Finite State Machine</td>
</tr>
<tr>
<td>GALS</td>
<td>Globally Asynchronous Locally Synchronous</td>
</tr>
<tr>
<td>GDB</td>
<td>GNU DeBugger</td>
</tr>
<tr>
<td>GDS</td>
<td>Graphical Data System</td>
</tr>
<tr>
<td>HDL</td>
<td>Hardware Description Language</td>
</tr>
<tr>
<td>ICE</td>
<td>In Circuit Emulator</td>
</tr>
<tr>
<td>IP</td>
<td>Intellectual Property</td>
</tr>
<tr>
<td>IPTG</td>
<td>Intellectual Property Traffic Generator</td>
</tr>
<tr>
<td>ISS</td>
<td>Instruction Set Simulator</td>
</tr>
<tr>
<td>JTAG</td>
<td>Joint Test Action Group</td>
</tr>
<tr>
<td>Abbreviation</td>
<td>Definition</td>
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<td>-------------------------------------------------</td>
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<tr>
<td>LCD</td>
<td>Liquid Crystal Display</td>
</tr>
<tr>
<td>LGI</td>
<td>Loose Generator Interface</td>
</tr>
<tr>
<td>LMI</td>
<td>Local Memory Interface</td>
</tr>
<tr>
<td>MDA</td>
<td>Model Driven Architecture</td>
</tr>
<tr>
<td>MMU</td>
<td>Memory Management Unit</td>
</tr>
<tr>
<td>NoC</td>
<td>Network on Chip</td>
</tr>
<tr>
<td>NUMA</td>
<td>Non-Uniform Memory Architecture</td>
</tr>
<tr>
<td>OS</td>
<td>Operating System</td>
</tr>
<tr>
<td>OSCI</td>
<td>Open SystemC Initiative</td>
</tr>
<tr>
<td>PC</td>
<td>Program Counter</td>
</tr>
<tr>
<td>PCI</td>
<td>Peripheral Component Interconnect</td>
</tr>
<tr>
<td>POSIX</td>
<td>Portable Operating System for unIX</td>
</tr>
<tr>
<td>RDB</td>
<td>Relational Data Base</td>
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<tr>
<td>RISC</td>
<td>Reduced Instruction Set Computer</td>
</tr>
<tr>
<td>ROM</td>
<td>Read Only Memory</td>
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<tr>
<td>RPC</td>
<td>Remote Procedure Call</td>
</tr>
<tr>
<td>RTL</td>
<td>Register Transfer Level</td>
</tr>
<tr>
<td>SAT</td>
<td>Satisfiability problem</td>
</tr>
<tr>
<td>SCE-MI</td>
<td>Standard Co-Emulation Modeling Interface</td>
</tr>
<tr>
<td>SCV</td>
<td>SystemC Verification</td>
</tr>
<tr>
<td>SDI</td>
<td>Streaming Data Interface</td>
</tr>
<tr>
<td>SEP</td>
<td>STBus External Port</td>
</tr>
<tr>
<td>SMP</td>
<td>Symmetric Multiprocessor Servers</td>
</tr>
<tr>
<td>SoC</td>
<td>System-on-Chip</td>
</tr>
<tr>
<td>SPAG</td>
<td>SysProbe Analysis Generator</td>
</tr>
<tr>
<td>SPES</td>
<td>SysProbe Embedded Software</td>
</tr>
<tr>
<td>SPIRIT</td>
<td>Structure for Packaging, Integrating and Re-using IP</td>
</tr>
<tr>
<td></td>
<td>within Tool-flows</td>
</tr>
<tr>
<td>SQL</td>
<td>Simple Query Language</td>
</tr>
<tr>
<td>SRAM</td>
<td>Static Random Access Memory</td>
</tr>
<tr>
<td>TLM</td>
<td>Transaction Level Modeling</td>
</tr>
<tr>
<td>UART</td>
<td>Universal Asynchronous Receiver and Transceiver</td>
</tr>
<tr>
<td>UML</td>
<td>Unified Modeling Language</td>
</tr>
<tr>
<td>VLIW</td>
<td>Very Long Instruction Word</td>
</tr>
<tr>
<td>VLNV</td>
<td>Vendor Library Name Version</td>
</tr>
<tr>
<td>XML</td>
<td>eXtensible Markup Language</td>
</tr>
<tr>
<td>XSD</td>
<td>XML Schema Definition</td>
</tr>
<tr>
<td>XSL</td>
<td>Extensible Stylesheet Language</td>
</tr>
</tbody>
</table>
Index

Abstraction level
  bus cycle accurate, BCA 12, 33, 108, 222
  register transfer, RTL 4, 24
  temporal 26
  timed, PVT 33, 106
  untimed, PV 33, 106
ARM 129, 140
Assertion 194

Bus functional model
  AXI 168
  OCP 168
  STBus 169

Co-design
  hardware 97
  hardware/software 96
  software 97
Co-emulation
  cycle accurate interface 184
  in-circuit 135, 178
  proxy 185
  SCE-MI 186
  self-test bench 183
  SPIRIT 254
  TLM 187
  transactional interface 179
  transactor 186

Communication
  arbiter 79
  channel 29
  initiator 29
  interconnect 29
  master 29
  port 29
  router 79
  slave 29
  synchronization 29
  target 29
Co-simulation
  SPIRIT 256
Co-verification 25
Cross-compilation 109

Debug
  transaction-based 215
Determinism 38
Device drivers 118
DUT
  reference model 156
  RTL 156
Endianness 110
Example
  ADSL modem 180
  I2C 125
  LCMPEG co-emulation 188
  MPEG4 codec 176
  set-top-box 236
SPI 126
TLM DMAC PL080 89
TLM MPEG4 codec 79
UART 99, 128

Firmware 119, 131
Functional verification 13

Golden model 158

Instruction-set simulator 230
Interrupt 39, 119, 133
ISS 25, 109

JTAG 137, 147

Linux 139

Micro-architectural features modeling 50
Micro-architecture 207
MMU See Virtual memory
Model equivalence
formal 185
memory dump 160
self-checking test 160
trace comparison 160
transaction comparison 216

Model of Computation 34, 47

Modeling concepts
bit-true behavior 30
communication delay 44
computational delay 44
functional delay 40
module 29
port 29
processes 29
register accurate 30
system synchronization 29
thread 29
time-annotated model 91
transaction 29

Modeling concepts standalone-timed model 44

Modeling environment
netlist assembly tool 62
system level debugger 62
transactional visualization 63

Modeling languages
C++ 58
synchronous languages 60
SystemC 61
SystemVerilog 61
Monitor 209
Multi-processor 21, 147

Native compilation 124

Open SystemC Initiative See OSCI
Operating system 112
OSCI 13
OSCI TLM Interface
Core TLM interface 65
Protocol interface 65
tlm_blocking_put_if 66
tlm_nonblocking_put_if 66
tlm_transport_if 66

Partitioning (hardware/software) 15
Performance
bandwidth 214
FIFO 224
latency 106, 209
memory controller 231
profiling 111
statistics 216
throughput 214
Polling 120
Process execution
determinism 38
Properties 191

Real-time 208
Real-time constraints 208

Shared memory 148, 208
SPIRIT
API 255
architecture analysis 207
editor 259
LGI 261
STBus 263
Static analysis tools
HPIOM 192, 196
LESAR 192
LUSSY 192
Synchronization 35
Index

SystemC
  notify 200
  process 200
  SC_THREAD 70
  scheduling policy 198
  template 73
  wait 71, 122, 194
SystemC verification library (SCV) 215, 223
System-on-chip 2

Test
  register tests 263
Test bench
  bus functional model 168
  IP 162
  monitor 171
  scenario 174
  system 163
Test data 159
Timed TLM 43
Timing
  hazards 104
  profiling 106
  resource overflow 105
  software correctness 104

TLM protocols
  TLM_STBUS 66
  TLM_SYNCHRO 66
  TLM_TAC 66
Traffic generator 222
Transaction 159
Transactional debug 209

Untimed TLM 33

VCC 11
Virtual memory 138
VLNV
  bus definition 243
  bus interface 244, 247
  design 245

XML
  design representation 249
  DOM 246
  multi-view 248
  parser 256
  SPIRIT 242
  Xerces 252
  XSD 253