

# List of Publications

- [1] Alexander Biedermann and Sorin A. Huss. *Selbstheilende Strukturen in einem virtualisierbaren eingebetteten MPSoC* IBM Academic Lab Days, Böblingen, Germany, November 2013.
- [2] Alexander Biedermann, Boris Dreyer and Sorin A. Huss. *A Generic, Scalable Reconfiguration Infrastructure for Sensor Networks Functionality Adaption*. 26th IEEE International SoC Conference (SOCC), Nürnberg, Germany, September 2013.
- [3] Alexander Biedermann and Sorin A. Huss. *A Methodology for Invasive Programming on Virtualizable Embedded MPSoC Architectures*. 13th International Conference on Computational Science (ICCS), Barcelona, Spain, June 2013.
- [4] Alexander Biedermann and Sorin A. Huss. *Hardware Virtualization-driven Software Task Switching in Reconfigurable Multi-Processor System-on-Chip Architectures*. ACM 5th Workshop on Mapping of Applications to MPSoCs (Map2MPSoC/SCOPEs 2012), St. Goar, Germany, May 2012.
- [5] Alexander Biedermann, Matthias Zöllner and Sorin A. Huss. *Automatic Code Parallelization and Architecture Generation for Embedded MPSoC*. ACM 5th Workshop on Mapping of Applications to MPSoCs (Map2MPSoC/SCOPEs 2012), St. Goar, Germany, May 2012.
- [6] Alexander Biedermann and Sorin A. Huss. *FripGa: A Prototypical Design Tool for Embedded Multi-Core System-on-Chip Architectures*. IEEE/ACM Design, Automation and Test in Europe, DATE'12, University Booth, Dresden Germany, March 2012.
- [7] Alexander Biedermann and Sorin A. Huss. *Scalable Multi-Core Virtualization for Embedded System-on-Chip Architectures*. IEEE/ACM Design, Automation and Test in Europe, DATE'12, Friday Workshop: Quo Vadis, Virtual Platforms? Dresden, Germany, January 2012.
- [8] Alexander Biedermann, Thorsten Piper, Lars Patzina, Sven Patzina, Sorin A Huss, Andy Schürr and Neeraj Suri. *Enhancing FPGA Robustness via Generic Monitoring IP Cores*. International Conference on Pervasive and Embedded Computing and Communication Systems, Vilamoura, Portugal, March 2011.
- [9] Alexander Biedermann, Marc Stoettinger, Lijing Chen and Sorin A. Huss. *Secure Virtualization within a Multi-Processor Soft-core System-on-Chip Architecture*. The 7th

International Symposium on Applied Reconfigurable Computing, Belfast, UK, March 2011.

- [10] Alexander Biedermann and H. Gregor Molter (Eds.). *Design Methodologies for Secure Embedded Systems*, volume 78. of *Lecture Notes in Electrical Engineering*. Springer, Berlin, Germany, November 2010.
- [11] André Seffrin and Alexander Biedermann. *Cellular-Array Implementations of Bio-Inspired Self-Healing Systems: State of the Art and Future Perspectives*. *Design Methodologies for Secure Embedded Systems*, volume 78. of *Lecture Notes in Electrical Engineering*, Berlin, November 2010.
- [12] André Seffrin, Alexander Biedermann and Sorin A. Huss. *Tiny-Pi: A Novel Formal Method for Specification, Analysis, and Verification of Dynamic Partial Reconfiguration Processes*. 13th IEEE Forum on Specification and Design Languages (FDL 2010), Southampton, UK, September 2010.
- [13] Marc Stoettinger, Alexander Biedermann and Sorin A. Huss. *Virtualization within a Parallel Array of Homogeneous Processing Units*. 6th International Symposium on Applied Reconfigurable Computing, Bangkok, Thailand, March 2010.
- [14] Felix Madlener, Sorin A. Huss and Alexander Biedermann. *RecDEVS: A Comprehensive Model of Computation for Dynamically Reconfigurable Hardware Systems*. 4th IFAC Workshop on Discrete-Event System Design (DESDes'09), Gandia, Spain, October 2009.

# List of supervised Theses

## Master Theses, Diploma Theses, and Bachelor Theses

- [1] Randolph Lieding. *Dynamic Task Switching in a virtualizable Multi-Processor System*. Bachelor Thesis, TU Darmstadt, April 2014.
- [2] Antonio Gavino Casu. *Power-Optimierung von Soft-Core-Prozessor-Virtualisierung*. Bachelor Thesis, TU Darmstadt, December 2013.
- [3] Boris Dreyer. *Dynamisches Rekonfigurationsnetzwerk zur wechselseitigen Rekonfiguration heterogener, verteilter eingebetteter Systeme*. Master Thesis, TU Darmstadt, October 2013.
- [4] Andreas Rjasanow. *Selbsteilende Strukturen in virtualisierbaren Multiprozessor-System-on-Chip-Architekturen*. Master Thesis, TU Darmstadt, June 2013.
- [5] Steffen Fleckenstein. *Massiv-parallele Videofilterung für FPGA-Boards*. Bachelor Thesis, TU Darmstadt, April 2012.
- [6] Wei Lin. *Virtualisierung von Soft-Core-Prozessoren*. Diplomarbeit, TU Darmstadt, January 2012.
- [7] Matthias Zöllner. *Modellierung von Parallelisierungsstrukturen für sequenzielle Algorithmen in C*. Bachelor Thesis, TU Darmstadt, January 2012.
- [8] Tobias Rückelt. *Implementierung eines Sensorsystems als Beispielapplikation für generisches FPGA-Monitoring*. Bachelor Thesis, TU Darmstadt, July 2011.
- [9] Clemens Bergmann. *Design einer dynamisch rekonfigurierbaren FPGA-Architektur*. Bachelor Thesis, TU Darmstadt, May 2011.
- [10] Maik Görtz. *FripGa - Software zur Codegenerierung von Many-Core-Architekturen auf FPGAs*. Master Thesis, TU Darmstadt, March 2011.
- [11] Jan Post. *Implementierung und Evaluation eines massiv-parallelen Bildskalierungsfilters auf einem FPGA*. Bachelor Thesis, TU Darmstadt, February 2011.
- [12] Andreas Rjasanow and Gregor Rynkowski. *Verteilte Triple-Voted-TMR-Architektur auf FPGA-Boards*. Bachelor Thesis, TU Darmstadt, February 2010.

## Final Theses (“Studienarbeiten”) and Practical Courses

- [1] Matthias Zöllner. *Parallelisierungstechniken für sequentiellen Code*. Final Thesis, TU Darmstadt, February 2014.
- [2] Boris Dreyer. *Kommunikation in einem virtualisierbaren MPSoC*. Practical Course, TU Darmstadt, January 2014.
- [3] Boris Dreyer. *Entwurf eines JTAG-eACE-Players für Mikroprozessor-basierte Systeme*. Final Thesis, TU Darmstadt, November 2013.
- [4] Kevin Luck. *Ein virtualisierbares Automotive MPSoC*. Final Thesis, TU Darmstadt, May 2013.
- [5] Nicolas Eicke, Sebastian Funke, Kai Schwierczek and Markus Tasch. *Framework zur Modellierung verteilter, paralleler eingebetteter HW/SW-Designs*. Practical Course, TU Darmstadt, October 2012.
- [6] Wei Lin. *Ein skalierbares Multi-Processor System-on-Chip zur Taskvirtualisierung*. Practical Course, TU Darmstadt, October 2012.
- [7] Tobias Rückelt. *Graphischer Editor für Models of Computation*. Final Thesis, TU Darmstadt, October 2012.
- [8] Wei Lin. *Implementierung und HW/SW-Partitionierung eines skalierbaren, verteilten FIR-Filters*. Practical Course, TU Darmstadt, July 2012.
- [9] Kevin Luck. *Glue Logic für Board-zu-Board-Kommunikation*. Practical Course, TU Darmstadt, July 2012.
- [10] Antonio Gavino Casu, Kadir Inac, Randolph Lieding, Mischa Lundberg and Daniel Schneider. *Virtualisierung in eingebetteten Multi-Prozessor-Systemen*. Practical Course, TU Darmstadt, April 2012.
- [11] Michael Koch, Niels Ströher, Lucas Rothamel and Manuel Weiel. *Framework zur Modellierung verteilter, paralleler eingebetteter HW/SW-Designs*. Practical Course, TU Darmstadt, April 2012.
- [12] Andreas Rjasanow. *Generischer Monitoring-IP-Core für FPGAs*. Final Thesis, TU Darmstadt, April 2012.
- [13] Wei Lin. *Integration von partiell-dynamischer Rekonfiguration in High-Level Design Tools*. Practical Course, TU Darmstadt, January 2012.
- [14] Jan Post. *Implementierung eines HW-IP-Cores für schnelles Pixel-Resampling*. Final Thesis, TU Darmstadt, October 2011.

- 
- [15] Hieu Ha Chi, Dan Le, Do Thanh Tung and Binh Vu Duc. *Graphisches Tool für parallelisierte HW/SW-FPGA-Designs*. Practical Course, TU Darmstadt, September 2011.
- [16] Quoc Hien Dang, Johannes Decher, Thorsten Jacobi and Omid Pahlevan Sharif. *Graphisches Tool für parallelisierte HW/SW-FPGA-Designs*. Practical Course, TU Darmstadt, September 2011.
- [17] Michael Koch, Niels Ströher, Lucas Rothamel and Manuel Weiel. *Graphisches Tool für parallelisierte HW/SW-FPGA-Designs*. Practical Course, TU Darmstadt, September 2011.
- [18] Clemens Bergmann. *Attacken auf Android-Smartphones*. Practical Course, TU Darmstadt, June 2011.
- [19] Peter Glöckner, Amir Naseri, Johannes Simon and Matthias Zöllner. *Framework für massiv-parallele Systeme in heterogenen FPGA-Netzwerken*. Practical Course, TU Darmstadt, April 2011.
- [20] Christopher Huth. *Methodiken zur Bewertung der Güte von Security-USB-Token*. Practical Course, TU Darmstadt, October 2010.
- [21] Tobias Rückelt. *Entwicklung eines redundanten Temperatursensors*. Practical Course, TU Darmstadt, October 2010.
- [22] Christopher Huth. *Man-in-the-PC-Attacke auf einen Banking-USB-Stick*. Semesterarbeit, TU Darmstadt, July 2010.
- [23] Joel Njeukam. *Partielle Rekonfiguration für Virtex-5 FPGAs*. Practical Course, TU Darmstadt, April 2010.

# Bibliography

- [Abassi 2010] L. Abassi. *2010 Haiti Earthquake Damage 4*. online: [http://upload.wikimedia.org/wikipedia/commons/a/a2/2010\\_Haiti\\_earthquake\\_damage4.jpg](http://upload.wikimedia.org/wikipedia/commons/a/a2/2010_Haiti_earthquake_damage4.jpg), accessed 07/01/2014, 9:00 am, 2010. 177
- [Ackland 2000] B. Ackland, A. Anesko, D. Brinthaup, S.J. Daubert, A. Kalavade, J. Knobloch, E. Micca, M. Moturi, C.J. Nicol, J.H. O'Neill et al. *A single-chip, 1.6-billion, 16-b MAC/s multiprocessor DSP*. IEEE Journal of Solid-State Circuits, vol. 35, no. 3, pages 412–424, 2000. 2
- [Ajtai 1983] M. Ajtai, J. Komlós and E. Szemerédi. *An  $O(N \log N)$  Sorting Network*. In Proceedings of the Symposium on Theory of Computing (STOC), pages 1–9. ACM, 1983. 38
- [Ambric Inc. 2008] Ambric Inc. *Am2000 Family Massively Parallel Processor Array*. online: <http://web.archive.org/web/20080516200115/http://www.ambric.com/products/>, accessed 12/11/2013, 11:40 am, May 2008. 107
- [Amdahl 1967] G.M. Amdahl. *Validity of the single Processor Approach to achieving large Scale computing Capabilities*. In Proceedings of the April 18–20, 1967, Spring Joint Computer Conference, pages 483–485. ACM, 1967. 129
- [ARM 2010] ARM. *AMBA 4 AXI4-Stream Protocol*, 1.0 edition, 2010. 79
- [Arora 1990] S. Arora, T. Leighton and B. Maggs. *On-line Algorithms for Path Selection in a nonblocking Network*. In Proceedings of the twenty-second annual ACM Symposium on Theory of Computing, pages 149–158. ACM, 1990. 37
- [Barthe 2011] L. Barthe, L.V. Cargnini, P. Benoit and L. Torres. *The SecretBlaze: A configurable and cost-effective open-source soft-core Processor*. In Proceedings of International Symposium on Parallel and Distributed Processing Workshops and Phd Forum (IPDPSW), pages 310–313. IEEE, 2011. 8
- [Batcher 1968] K.E. Batcher. *Sorting Networks and their Applications*. In Proceedings of the April 30–May 2, 1968, Spring Joint Computer Conference, pages 307–314. ACM, 1968. 38
- [Beaumont 2012] M. Beaumont, B. Hopkins and T. Newby. *SAFER PATH: Security Architecture using fragmented Execution and Replication for Protection against trojaned*

- Hardware*. In Proceedings of the Conference on Design, Automation and Test in Europe (DATE), pages 1000–1005. EDA Consortium, 2012. 14
- [Beck 2001] K. Beck, M. Beedle, A. Van Bennekum, A. Cockburn, W. Cunningham, M. Fowler, J. Grenning, J. Highsmith, A. Hunt, R. Jeffries et al. *Manifesto for Agile Software Development*, 2001. 135
- [Belanovic 2003] P. Belanovic, M. Holzer, D. Micušik and M. Rupp. *Design Methodology of Signal Processing Algorithms in Wireless Systems*. In Proceedings of the International Conference on Computer, Communication and Control Technologies (CCCT), pages 288–291, 2003. 1, 2
- [Bell 2008] S. Bell, B. Edwards, J. Amann, R. Conlin, K. Joyce, V. Leung, J. MacKay, M. Reif, L. Bao, J. Brown et al. *Tile64-Processor: A 64-Core SoC with Mesh Interconnect*. In Proceedings of the International Solid-State Circuits Conference (ISSCC), pages 88–598. IEEE, 2008. 33
- [Benini 2002] L. Benini and G. De Micheli. *Networks on Chips: A new SoC Paradigm*. Computer, vol. 35, no. 1, pages 70–78, 2002. 33
- [Biedermann 2008] A. Biedermann and B. Meyer. *Theoretische und algorithmische Evaluation eines massiv-parallelen Multiprozessorarrays der Am2000-Familie unter Verwendung von Videoalgorithmen*. Diploma Thesis, TU Darmstadt, September 2008. 38, 107
- [Biedermann 2011a] A. Biedermann, T. Piper, L. Patzina, S. Patzina, S.A. Huss, A. Schürr and N. Suri. *Enhancing FPGA Robustness via Generic Monitoring IP Cores*. In Proceedings of International Conference on Pervasive Embedded Computing and Communication Systems (PECCS), pages 379–386, 2011. 96, 120, 163
- [Biedermann 2011b] A. Biedermann, M. Stoettinger, L. Chen and S.A. Huss. *Secure Virtualization within a Multi-Processor soft-core System-on-Chip Architecture*. In Proceedings of the International Symposium on Applied Reconfigurable Computing (ARC), pages 385–396. Springer, 2011. 17
- [Biedermann 2012a] A. Biedermann and S.A. Huss. *FripGa: A Prototypical Design Tool for Embedded Multi-Core System-on-Chip Architectures*. In Conference on Design, Automation and Test in Europe (DATE), University Booth. IEEE/ACM, 2012. 110
- [Biedermann 2012b] A. Biedermann and S.A. Huss. *Hardware Virtualization-driven Software Task Switching in Reconfigurable Multi-Processor System-on-Chip Architectures*. In Proceedings of the Workshop on Mapping of Applications to MPSoCs (Map2MPSoC/SCOPES), pages 32–41. ACM, 2012. 67

- [Biedermann 2012c] A. Biedermann and S.A. Huss. *Scalable Multi-Core Virtualization for Embedded System-on-Chip Architectures*. In Conference on Design, Automation and Test in Europe (DATE), Friday Workshop: Quo Vadis, Virtual Platforms? IEEE/ACM, 2012. 39
- [Biedermann 2012d] A. Biedermann, M. Zöllner and S.A. Huss. *Automatic Code Parallelization and Architecture Generation for Embedded MPSoC*. In Workshop on Mapping of Applications to MPSoCs (Map2MPSoC/SCOPES 2012), 2012. 123
- [Biedermann 2013a] A. Biedermann, B. Dreyer and S.A. Huss. *A Generic, Scalable Reconfiguration Infrastructure for Sensor Networks Functionality Adaption*. In International SoC Conference (SOCC). IEEE, 2013. 54
- [Biedermann 2013b] A. Biedermann and S.A. Huss. *A Methodology for Invasive Programming on Virtualizable Embedded MPSoC Architectures*. In Proceedings of International Conference on Computational Science (ICCS), pages 359–368. Procedia Computer Science, 2013. 135
- [Bolchini 2007] C. Bolchini, A. Miele and M.D. Santambrogio. *TMR and Partial Dynamic Reconfiguration to mitigate SEU faults in FPGAs*. In Proceedings of International Symposium on Defect and Fault-Tolerance in VLSI Systems (DFT), pages 87–95. IEEE, 2007. 121
- [Bonamy 2012] R. Bonamy, H.M. Pham, S. Pillement and D. Chillet. *Ultra-fast power-aware Reconfiguration Controller*. In Proceedings of Conference on Design, Automation and Test in Europe (DATE), pages 1373–1378. IEEE/ACM, 2012. 55
- [Brebner 1996] G.J. Brebner. *A Virtual Hardware Operating System for the Xilinx XC6200*. In Proceedings of Conference on Field-Programmable Logic and Applications (FPL), pages 327–336. Springer, 1996. 6
- [Brebner 2001] G.J. Brebner and O. Diessel. *Chip-Based reconfigurable Task Management*. In Proceedings of Conference on Field-Programmable Logic and Applications (FPL), pages 182–191. IEEE, 2001. 6
- [Burke 2004] E.K. Burke, P. De Causmaecker and G. Vanden Berghe. *Novel meta-heuristic Approaches to Nurse Rostering Problems in Belgian Hospitals*. Handbook of Scheduling: Algorithms, Models and Performance Analysis, vol. 18, pages 1–44, 2004. 67
- [Casu 2011] A.G. Casu, K. Inac, R. Lieding, M. Lundberg and D. Schneider. *Virtualisierung in eingebetteten Multi-Prozessor-Systemen*. Practical Course, TU Darmstadt, April 2011. 112
- [Casu 2013] A.G. Casu. *Power-Optimierung von Soft-Core-Prozessor-Virtualisierung*. Bachelor Thesis, TU Darmstadt, December 2013. 102, 180



- [Ceng 2008] J. Ceng, J. Castrillon, W. Sheng, H. Scharwächter, R. Leupers, G. Ascheid, H. Meyr, T. Isshiki and H. Kunieda. *MAPS: An integrated Framework for MPSoC Application Parallelization*. In Proceedings of the Annual Design Automation Conference (DAC), pages 754–759. ACM, 2008. 127
- [Cerone 2009] V. Cerone, M. Milanese and D. Regruto. *Combined automatic Lane-Keeping and Driver's Steering through a 2-DOF Control Strategy*. IEEE Transactions on Control Systems Technology, vol. 17, no. 1, pages 135–142, 2009. 152
- [Chakrabarty 2009] A. Chakrabarty, M. Collier and S. Mukhopadhyay. *Matrix-based Nonblocking Routing Algorithm for Beneš Networks*. In Proceedings of Conference on Future Computing, Service Computation, Cognitive, Adaptive, Content, Patterns (Computationworld), pages 551–556. IEEE, 2009. 37
- [Chandra 1997] R. Chandra, D.-K. Chen, R. Cox, D.E. Maydan, N. Nedeljkovic and J.M. Anderson. *Data Distribution Support on Distributed Shared Memory Multiprocessors*. ACM SIGPLAN Notices, vol. 32, no. 5, pages 334–345, 1997. 123
- [Chen 2007] T. Chen, R. Raghavan, J.N. Dale and E. Iwata. *Cell Broadband Engine Architecture and its first Implementation – A Performance View*. IBM Journal of Research and Development, vol. 51, no. 5, pages 559–572, 2007. 1, 32
- [Chen 2009] C.T. Chen and Y.S. Chen. *Real-time Approaching Vehicle Detection in Blind-Spot Area*. In Proceedings of 12th International IEEE Conference on Intelligent Transportation Systems (ITSC), pages 1–6. IEEE, 2009. 152
- [Clos 1953] C. Clos. *A Study of non-blocking Switching Networks*. Bell System Technical Journal, vol. 32, no. 2, pages 406–424, 1953. 34
- [Cohen 2010] A. Cohen and E. Rohou. *Processor Virtualization and split Compilation for heterogeneous Multicore Embedded Systems*. In Proceedings of Design Automation Conference (DAC), pages 102–107. ACM, 2010. 5
- [Cordes 2013] D. Cordes, O. Neugebauer, M. Engel and P. Marwedel. *Automatic Extraction of Task-Level Parallelism for Heterogeneous MPSoCs*. In Proceedings of International Conference on Parallel Processing (ICPP), pages 950–959. IEEE, 2013. 123
- [Cotret 2012] P. Cotret, J. Crenne, G. Gogniat and J. Diguët. *Bus-based MPSoC Security through Communication Protection: A latency-efficient Alternative*. In Proceedings of Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM), pages 200–207. IEEE, 2012. 95
- [Dagum 1998] L. Dagum and R. Menon. *OpenMP: An Industry Standard API for Shared-Memory Programming*. Computational Science & Engineering, IEEE, vol. 5, no. 1, pages 46–55, 1998. 123, 127

- [Darms 2006] M. Darms and H. Winner. *Umfelderfassung für ein Fahrerassistenzsystem zur Unfallvermeidung*. In VDI Berichte, volume 1931 of VDI, page 207, 2006. 150
- [Densmore 2006] D. Densmore and R. Passerone. *A Platform-based Taxonomy for ESL Design*. IEEE Design & Test of Computers, vol. 23, no. 5, pages 359–374, 2006. 109
- [Dkroetsch 2011] Dkroetsch. *Aeryon Scout with Camera*. online: [http://commons.wikimedia.org/wiki/File:Aeryon\\_Scout\\_With\\_Camera.jpg](http://commons.wikimedia.org/wiki/File:Aeryon_Scout_With_Camera.jpg), accessed 07/01/2014, 9:10 am, 04 2011. 173
- [Dreyer 2014] B. Dreyer. *Kommunikation in einem virtualisierbaren MPSoC*. Forschungsarbeit, TU Darmstadt, January 2014. 93
- [Eicke 2012] N. Eicke, S. Funke, K. Schwierczek and M. Tasch. *Framework zur Modellierung verteilter, paralleler eingebetteter HW/SW-Designs*. Practical Course, TU Darmstadt, October 2012. 69
- [Felzenszwalb 2004] P. Felzenszwalb and D. Huttenlocher. *Efficient graph-based Image Segmentation*. International Journal of Computer Vision, vol. 59, no. 2, pages 167–181, 2004. 175
- [Ferber 2012] M. Ferger, M.A. Kadi, M. Hubner, M. Koedam, S. Sinha, K. Goossens, G.M. Almeida, J.R. Azambuja and J. Becker. *Hardware / Software Virtualization for the Reconfigurable Multicore Platform*. In Proceedings of the International Conference on Computational Science and Engineering (CSE), pages 341–344. IEEE, 2012. 6
- [Figuli 2011] P. Figuli, M. Hubner, R. Girardey, F. Bapp, T. Bruckschlogl, F. Thoma, J. Henkel and J. Becker. *A heterogeneous SoC Architecture with embedded virtual FPGA Cores and runtime Core Fusion*. In Proceedings of Conference on Adaptive Hardware and Systems (AHS), pages 96–103. NASA/ESA, 2011. 6
- [Franke 2003] B. Franke and M.F.P. Oboyle. *Compiler Parallelization of C Programs for multi-core DSPs with multiple Address Spaces*. In Proceedings of International Conference on Hardware/Software Codesign and System Synthesis, pages 219–224. IEEE/ACM/IFIP, 2003. 123
- [Ganssle 2008] Jack Ganssle. *The Nulticore Effect*. online: <http://www.embedded.com/design/mcus-processors-and-socs/4008183/The-Nulticore-effect>, accessed 11/06/2013, 2:15 pm, 2008. 2
- [Gericota 2005] M.G. Gericota, G.R. Alves and J.M. Ferreira. *A self-healing Real-Time System based on run-time Self-Reconfiguration*. In Proceedings of Conference on Emerging Technologies and Factory Automation (ETFA), volume 1, pages 4–pp. IEEE, 2005. 116

- [Glöckner 2011] P. Glöckner, A. Naseri, J. Simon and M. Zöllner. *Framework für massiv-parallele Systeme in heterogenen FPGA-Netzwerken*. Practical Course, TU Darmstadt, April 2011. 112
- [Goke 1973] L. Rodney Goke and G.J. Lipovski. *Banyan Networks for partitioning Multiprocessor Systems*. ACM SIGARCH Computer Architecture News, vol. 2, no. 4, pages 21–28, 1973. 34
- [Goldberg 1974] R.P. Goldberg. *Survey of virtual Machine Research*. Computer, vol. 7, no. 6, pages 34–45, 1974. 5
- [Green 2013] O. Green and Y. Birk. *Scheduling Directives for shared-memory Many-Core Processor Systems*. In Proceedings of the International Workshop on Programming Models and Applications for Multicores and Manycores, pages 115–124. ACM, 2013. 57
- [Görtz 2011] M. Görtz. *FripGa - Software zur Codegenerierung von Many-Core-Architekturen auf FPGAs*. Master Thesis, TU Darmstadt, March 2011. 112
- [Haase 2004] J. Haase, F. Eschmann, B. Klauer and K. Waldschmidt. *The SDVM: A self distributing Virtual Machine*. In Proceedings of International Conference on Architecture of Computing Systems (ARCS), volume 2981, 2004. 5
- [Hansson 2011] A. Hansson, M. Ekerhult, A. Molnos, A. Milutinovic, A. Nelson, J. Ambrose and K. Goossens. *Design and Implementation of an Operating System for Composable Processor Sharing*. Microprocessors and Microsystems, vol. 35, no. 2, pages 246–260, 2011. 6
- [Hübner 2006] M. Hübner, C. Schuck, M. Kühnle and J. Becker. *New 2-dimensional partial dynamic Reconfiguration Techniques for real-time adaptive Microelectronic Circuits*. In Proceedings of Annual Symposium on Emerging VLSI Technologies and Architectures, pages 6–pp. IEEE, 2006. 54
- [Heiser 2008] G. Heiser. *The Role of Virtualization in Embedded Systems*. In Proceedings of Workshop on Isolation and Integration in Embedded Systems (IIES), pages 11–16. ACM, 2008. 5
- [Hemani 2000] A. Hemani, A. Jantsch, S. Kumar, A. Postula, J. Oberg, M. Millberg and D. Lindqvist. *Network on Chip: An Architecture for Billion Transistor Era*. In Proceedings of the NorChip Conference, volume 31. IEEE, 2000. 33
- [Henkel 2003] J. Henkel. *Closing the SoC Design Gap*. Computer, vol. 36, no. 9, pages 119–121, 2003. 1
- [Henkel 2012] J. Henkel, A. Herkersdorf, L. Bauer, T. Wild, M. Hubner, Ravi K. Pujari, A. Grudnitsky, J. Heisswolf, A. Zaib, B. Vogel et al. *Invasive Manycore Architec-*

- tures. In Proceedings of Asia and South Pacific Design Automation Conference (ASP-DAC), pages 193–200. IEEE, 2012. 33, 135
- [Hofmann 2008] A. Hofmann and K. Waldschmidt. *SDVM^R: A Scalable Firmware for FPGA-Based Multi-core Systems-on-Chip*. In Proceedings of Annual Symposium on VLSI (ISVLSI), pages 387–392. IEEE, 2008. 6
- [Howard 2010] J. Howard, S. Dighe, Y. Hoskote, S. Vangal, D. Finan, G. Ruhl, D. Jenkins, H. Wilson, N. Borkar, G. Schrom et al. *A 48-Core IA-32 message-passing Processor with DVFS in 45nm CMOS*. In Proceedings of International Solid-State Circuits Conference (ISSCC), pages 108–109. IEEE, 2010. 33
- [Huang 2009] C.H. Huang and P.-A. Hsiung. *Hardware Resource Virtualization for dynamically partially reconfigurable Systems*. IEEE Embedded Systems Letters, vol. 1, no. 1, pages 19–23, 2009. 6
- [Intel Corporation 2011] Intel Corporation. *Intel Refreshes Ultimate Enthusiast Processor Lineup with Six-Core Offerings*. online: [http://newsroom.intel.com/community/intel\\_newsroom/blog/2011/11/14/intel-refreshes-ultimate-enthusiast-processor-lineup-with-six-core-offerings](http://newsroom.intel.com/community/intel_newsroom/blog/2011/11/14/intel-refreshes-ultimate-enthusiast-processor-lineup-with-six-core-offerings), accessed 11/28/2013, 3:00 pm, 2011. 7
- [Intel Corporation 2013a] Intel Corporation. *Desktop 3rd Generation Intel Core Processor Family, Desktop Intel Pentium Processor Family, Desktop Intel Celeron Processor Family, and LGA1155 Socket Thermal Mechanical Specifications and Design Guidelines (TMSDG)*. Intel Corporation, 1 2013. 7
- [Intel Corporation 2013b] Intel Corporation. *Intel64 and IA-32 Architectures Software Developer's Manual*. Intel Corporation, vol. 2 edition, 3 2013. 7
- [Irwin 2004] M.J. Irwin, L. Benini, N. Vijaykrishnan and M. Kandemir. *Techniques for designing energy-aware MPSoCs*, pages 21–47. Morgan Kaufman, 2004. 102
- [Israr 2012] A. Israr. *Reliability Aware High-Level Embedded System Design in presence of Hard and Soft Errors*. PhD Thesis, TU Darmstadt, May 2012. 117, 118, 154, 156
- [Jozwik 2012] K. Jozwik, H. Tomiyama, M. Edahiro, S. Honda and H. Takada. *Comparison of Preemption Schemes for Partially Reconfigurable FPGAs*. IEEE Embedded Systems Letters, vol. 4, no. 2, pages 45–48, 2012. 6
- [Jung 2005] H.G. Jung, D.S. Kim, P.J. Yoon and J.H. Kim. *Computer Analysis of Images and Patterns*, chapter Stereo Vision based Localization of free Parking Site, pages 231–239. Springer, 2005. 152
- [Kalte 2005] H. Kalte and M. Porrmann. *Context Saving and Restoring for Multitasking in reconfigurable Systems*. In Proceedings of Conference on Field-Programmable Logic and Applications (FPL), pages 223–228. IEEE, 2005. 14

- [Khronos OpenCL Working Group 2008] Khronos OpenCL Working Group. *The OpenCL Specification*. A. Munshi (ed.), 2008. 123
- [Kistler 2006] M. Kistler, M. Perrone and F. Petrini. *Cell Multiprocessor Communication Network: Built for Speed*. IEEE Micro, vol. 26, no. 3, pages 10–23, 2006. 78
- [Knuth 1997] D.E. Knuth. *The Art of Computer Programming*, volume 3: Sorting and Searching, chapter 5.3.4: Networks for Sorting, pages 219–247. Addison-Wesley, 1997. 38
- [Koal 2013] T. Koal, M. Ulbricht and H.T. Vierhaus. *Virtual TMR Schemes Combining Fault Tolerance and Self Repair*. In Proceedings of Conference on Digital System Design (DSD), pages 235–242. Euromicro, 2013. 119
- [Koch 2011] M. Koch, N. Ströher, L. Rothamel and M. Weiel. *Graphisches Tool für parallelisierte HW/SW-FPGA-Designs*. Practical Course, TU Darmstadt, September 2011. 112
- [Koch 2012] M. Koch, N. Ströher, L. Rothamel and M. Weiel. *Framework zur Modellierung verteilter, paralleler eingebetteter HW/SW-Designs*. Forschungsarbeit, TU Darmstadt, April 2012. 112
- [Kopetz 2008] H. Kopetz, C. El Salloum, B. Huber, R. Obermaisser and C. Paukovits. *Composability in the Time-triggered System-on-Chip Architecture*. In International System-on-Chip Conference (SOC), pages 87–90. IEEE, 2008. 5
- [Kuck 1981] D.J. Kuck, R.H. Kuhn, D.A. Padua, B. Leasure and M. Wolfe. *Dependence Graphs and Compiler Optimizations*. In Proceedings of the ACM SIGPLAN-SIGACT Symposium on Principles of Programming Languages, pages 207–218. ACM, 1981. 125
- [Lala 2003] P.K. Lala and B.K. Kumar. *An Architecture for self-healing Digital Systems*. Journal of Electronic Testing, vol. 19, no. 5, pages 523–535, 2003. 116
- [Lanuzza 2009] M. Lanuzza, P. Zicari, F. Frustaci, S. Perri and P. Corsonello. *An efficient and low-cost Design Methodology to improve SRAM-based FPGA Robustness in Space and Avionics Applications*. In Proceedings of the International Symposium on Applied Reconfigurable Computing, pages 74–84. Springer, 2009. 54
- [Leiserson 2010] C.E. Leiserson. *The Cilk++ Concurrency Platform*. The Journal of Supercomputing, vol. 51, no. 3, pages 244–257, 2010. 123
- [Leu 2011] A. Leu, D. Aiteanu and A. Graser. *A novel stereo Camera based Collision Warning System for Automotive Applications*. In Proceedings of International Symposium on Applied Computational Intelligence and Informatics (SACI), pages 409–414. IEEE, 2011. 152

- [Leupers 2012] R. Leupers, G. Martin, R. Plyaskin, A. Herkersdorf, F. Schirrmeister, T. Kogel and M. Vaupel. *Virtual Platforms: Breaking new Grounds*. In Proceedings of the Conference on Design, Automation and Test in Europe (DATE), pages 685–690. EDA Consortium, 2012. 6
- [Levinson 2000] L. Levinson, R. Manner, M. Sessler and H. Simmler. *Preemptive Multi-tasking on FPGAs*. In Symposium on Field-Programmable Custom Computing Machines, pages 301–302. IEEE, 2000. 14
- [Lieding 2014] R. Lieding. *Dynamic Task Mapping in a virtualizable Multi-Processor System*. Bachelor Thesis, TU Darmstadt, March 2014. 180
- [Lin 2012] W. Lin. *Virtualisierung von Soft-Core-Prozessoren*. Diplomarbeit, TU Darmstadt, January 2012. 38
- [Liu 1993] J. Liu and V.A. Saletore. *Self-scheduling on distributed-memory Machines*. In Proceedings of the Conference on Supercomputing, pages 814–823. ACM/IEEE, 1993. 67
- [Luck 2013] K. Luck. *Ein virtualisierbares Automotive MPSoC*. Final Thesis, TU Darmstadt, May 2013. 152
- [Marwedel 2011] P. Marwedel, J. Teich, G. Kouveli, J. Bacivarov, L. Thiele, S. Ha, C. Lee, Q. Xu and L. Huang. *Mapping of Applications to MPSoCs*. In Proceedings of the International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), pages 109–118. IEEE, 2011. 118
- [Meloni 2010] P. Meloni, S. Secchi and L. Raffo. *An FPGA-based Framework for technology-aware Prototyping of multicore embedded Architectures*. IEEE Embedded Systems Letters, vol. 2, no. 1, pages 5–9, 2010. 112
- [Mentor Graphics 2013] Mentor Graphics. *ModelSim - Leading Simulation and Debugging*. online: <http://www.mentor.com/products/fpga/model>, accessed 12/18/2013, 10:10 am, 2013. 112
- [Momtazpour 2011] M. Momtazpour, M. Ghorbani, M. Goudarzi and E. Sanaei. *Simultaneous variation-aware Architecture Exploration and Task Scheduling for MPSoC Energy Minimization*. In Proceedings of the Great Lakes Symposium on VLSI, pages 271–276. ACM, 2011. 75
- [Moore 1965] G.E. Moore et al. *Cramming more Components onto Integrated Circuits*, 1965. 1
- [Muller 2013] S. Muller, M. Scholzel and H.T. Vierhaus. *Towards a Graceful Degradable Multicore-System by Hierarchical Handling of Hard Errors*. In Proceedings of International Conference on Parallel, Distributed and Network-Based Processing (PDP), pages 302–309. Euromicro, 2013. 117

- [Nassimi 1981] D. Nassimi and S. Sahni. *A Self-Routing Benes Network and Parallel Permutation Algorithms*. IEEE Transactions on Computers, vol. C-30, no. 5, pages 332–340, 1981. 37
- [Nvidia 2011] Nvidia. *NVIDIA CUDA Programming Guide*, 2011. 123
- [Otoni 2005] G. Otoni, R. Rangan, A. Stoler and D.I. August. *Automatic Thread Extraction with decoupled Software Pipelining*. In Proceedings of International Symposium on Microarchitecture (MICRO), pages 12 pp.–. IEEE/ACM, 2005. 123
- [Parberry 1992] I. Parberry. *The pairwise Sorting Network*. Parallel Processing Letters, vol. 2, no. 2, page 3, 1992. 38
- [Patel 1981] J.H. Patel. *Performance of Processor-Memory Interconnections for Multiprocessors*. IEEE Transactions on Computers, vol. C-30, no. 10, pages 771–780, 1981. 34
- [Paulsson 2006a] K. Paulsson, M. Hubner and J. Becker. *Strategies to On-Line Failure Recovery in Self-Adaptive Systems based on dynamic and partial Reconfiguration*. In Proceedings of NASA/ESA Conference on Adaptive Hardware and Systems (AHS), pages 288–291. NASA/ESA, 2006. 121
- [Paulsson 2006b] K. Paulsson, M. Hubner, M. Jung and J. Becker. *Methods for runtime Failure Recognition and Recovery in dynamic and partial reconfigurable Systems based on Xilinx Virtex-II Pro FPGAs*. In Proceedings of Annual Symposium on Emerging VLSI Technologies and Architectures, pages 6–pp. IEEE, 2006. 54, 167
- [Pionteck 2006] T. Pionteck, R. Koch and C. Albrecht. *Applying partial Reconfiguration to Networks-on-Chips*. In International Conference on Field-Programmable Logic (FPL), pages 1–6. IEEE, 2006. 56
- [Plurality 2013] Plurality. *Plurality - Leading the Multicore Revolution*. online: <http://www.plurality.com/technology.html>, accessed: 12/16/2013, 11:15 am, 2013. 57
- [Polychronopoulos 1987] C.D. Polychronopoulos and D.J. Kuck. *Guided Self-Scheduling: A Practical Scheduling Scheme for Parallel Supercomputers*. IEEE Transactions on Computers, vol. C-36, no. 12, pages 1425–1439, 1987. 67
- [Portland Business Journal 2008] Portland Business Journal. *Ambric for sale*. online: <http://www.bizjournals.com/portland/stories/2008/11/17/daily25.html?t=printable>, accessed 12/11/2013, 11:50 am, November 2008. 107
- [Post 2011] J. Post. *Implementierung und Evaluation eines massiv-parallelen Bildskalierungsfilters auf einem FPGA*. Bachelor Thesis, TU Darmstadt, February 2011. 113

- [Quinlan 2011] D.J. Quinlan and C. Liao. *ROSE Source-to-Source Compiler Infrastructure*. In Proceedings of Cetus Users and Compiler Infrastructure Workshop in conjunction with PACT, volume 2011, page 1, 2011. 127
- [Rückelt 2011] T. Rückelt. *Implementierung eines Sensorsystems als Beispielapplikation für generisches FPGA-Monitoring*. Bachelor Thesis, TU Darmstadt, July 2011. 120
- [Rückelt 2012] T. Rückelt. *Graphischer Editor für Models of Computation*. Final Thesis, TU Darmstadt, October 2012. 112
- [Research 2006] CORDIS Community Research and Development Information Service. *Information Society Technologies - Facts & Figures: Hardware*. online: <http://cordis.europa.eu/ist/embedded/hardware.htm>, accessed 11/01/2013, 9:30 am, July 2006. 7
- [Rjasanow 2012] A. Rjasanow. *Generischer Monitoring-IP-Core für FPGAs*. Final Thesis, TU Darmstadt, April 2012. 120
- [Rjasanow 2013] A. Rjasanow. *Selbsteilende Strukturen in virtualisierbaren Multiprozessor-System-on-Chip-Architekturen*. Master Thesis, TU Darmstadt, June 2013. 100
- [Rudolph 1985] L. Rudolph. *A Robust Sorting Network*. IEEE Transactions on Computers, vol. C-34, no. 4, pages 326–335, 1985. 38
- [Runge 2012] A. Runge. *Determination of the Optimum Degree of Redundancy for Fault-prone Many-Core Systems*. GMM-Fachbericht Zuverlässigkeit und Entwurf, 2012. 120
- [Seebach 2010] H. Seebach, F. Nafz, J. Holtmann, J. Meyer, M. Tichy, W. Reif and W. Schäfer. *Designing Self-Healing in automotive Systems*. In Proceedings of Conference on Autonomic and Trusted Computing (ATC), pages 47–61. Springer, 2010. 120
- [Seffrin 2010] A. Seffrin and A. Biedermann. *Cellular-Array Implementations of Bio-Inspired Self-Healing Systems: State of the Art and Future Perspectives*. In Design Methodologies for Secure Embedded Systems, volume 78 of *Lecture Notes in Electrical Engineering*, pages 151–170, Berlin, 2010. Springer. 116
- [Sidiropoulos 2013] H. Sidiropoulos, P. Figuli, K. Siozios, D. Soudris and J. Becker. *A Platform-independent runtime Methodology for mapping multiple Applications onto FPGAs through Resource Virtualization*. In Proceedings of Conference on Field-Programmable Logic and Applications (FPL), pages 1–4. IEEE, 2013. 6
- [Simmler 2000] H. Simmler, L. Levinson and R. Männer. *Multitasking on FPGA Coprocessors*. In Proceedings of Conference on Field-Programmable Logic and Applications (FPL), pages 121–130. IEEE, 2000. 6



- [Singh 2013] A.K. Singh, M. Shafique, A. Kumar, J. Henkel, A. Das, W. Jigang, T. Srikanthan, S. Kaushik, Y. Ha, A. Prakash et al. *Mapping on multi/many-core Systems: Survey of current and emerging Trends*. In Proceedings of the International Conference on Computer-Aided Design (ICCAD), pages 508–515. IEEE/ACM, 2013. 118
- [Stoettinger 2010] M. Stoettinger, A. Biedermann and S.A. Huss. *Virtualization within a Parallel Array of Homogeneous Processing Units*. In Proceedings of the International Symposium on Applied Reconfigurable Computing (ARC), pages 17–28, 2010. 6
- [Sunderam 1990] V.S. Sunderam. *PVM: A Framework for parallel distributed Computing*. Concurrency: Practice and Experience, vol. 2, no. 4, pages 315–339, 1990. 5
- [Tang 1986] P. Tang and P.-C. Yew. *Processor Self-Scheduling for Multiple-Nested Parallel Loops*. In Proceedings of International Conference on Parallel Processing (ICPP), volume 86, pages 528–535, 1986. 67
- [Tcl Developer Xchange 2013] Tcl Developer Xchange. *Welcome to the Tcl Developer Xchange!* online: <http://www.tcl.tk/>, accessed: 13/11/2013, 13:00 am, 2013. 111
- [Teich 2008] J. Teich. *Invasive Algorithms and Architectures*. In it - Information Technology, volume 50, No. 5, pages 300–310, 2008. 135
- [Teich 2012] J. Teich, A. Weichslgartner, B. Oechslein and W. Schroder-Preikschat. *Invasive Computing - Concepts and Overheads*. In Proceedings of the Forum on Specification and Design Languages (FDL), pages 217–224. ECSI, 2012. 135
- [Ullmann 2004] M. Ullmann, M. Hübner, B. Grimm and J. Becker. *On-demand FPGA runtime System for dynamical Reconfiguration with adaptive Priorities*. In Proceedings of Conference on Field-Programmable Logic and Applications (FPL), pages 454–463. IEEE, 2004. 54
- [Varanasi 2011] P. Varanasi and G. Heiser. *Hardware-supported Virtualization on ARM*. In Proceedings of the Second Asia-Pacific Workshop on Systems, page 11. ACM, 2011. 5
- [Vector Fabrics 2013] Vector Fabrics. *Pareon*. online: <http://www.vectorfabrics.com/products>, 2013. 127
- [Ventroux 2005] N. Ventroux and F. Blanc. *A low complex Scheduling Algorithm for Multi-Processor System-on-Chip*. In Proceedings of the Conference on Parallel and Distributed Computing and Networks, pages 540–545. IASTED/ACTA Press, 2005. 75
- [Waksman 1968] A. Waksman. *A Permutation Network*. Journal of the ACM, vol. 15, no. 1, pages 159–163, 1968. 34

- [Wichman 2006] S. Wichman, S. Adyha, S. Ahrens, R. Ambli, B. Alcorn, D. Connors and D. Fay. *Partial Reconfiguration across FPGAs*. In Proceedings of the Military and Aerospace Applications of Programmable Logic Devices and Technologies Conference, pages 26–28, 2006. 54
- [Wirth 1995] N. Wirth. *A Plea for lean Software*. Computer, vol. 28, no. 2, pages 64–68, 1995. 1
- [Wolf 2008] W. Wolf, A.A. Jerraya and G. Martin. *Multiprocessor System-on-Chip (MPSoC) Technology*. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 27, no. 10, pages 1701–1713, 2008. 2
- [Wu 2009] J. Wu, M. Si, F. Tan and C. Gu. *Real-time automatic Road Sign Detection*. In Proceedings of International Conference on Image and Graphics (ICIG), pages 540–544. IEEE, 2009. 152
- [Xilinx, Inc. 2011] Xilinx, Inc. *LogiCORE IP Fast Simplex Link (FSL) V2o Bus (v2.11e)*. Xilinx, Inc., Oct. 2011. 79
- [Xilinx, Inc. 2012] Xilinx, Inc. *MicroBlaze Processor Reference Guide*. Xilinx, Inc., v14.1 edition, 04 2012. 7, 80, 85
- [Xilinx, Inc. 2013a] Xilinx, Inc. *MicroBlaze Soft Processor Core*. online: <http://www.xilinx.com/tools/microblaze.htm>, accessed: 10/01/2013, 11:45 am, 2013. 9
- [Xilinx, Inc. 2013b] Xilinx, Inc. *PicoBlaze 8-bit Microcontroller*. online: <http://www.xilinx.com/products/intellectual-property/picoblaze.htm>, accessed: 10/01/2013, accessed 11:55 am, 2013. 8
- [Xilinx, Inc. 2013c] Xilinx, Inc. *Vivado Design Suite*. online: <http://www.xilinx.com/products/design-tools/vivado/>, accessed 12/18/2013, 10:45 am, 2013. 109
- [Yamauchi 1996] T. Yamauchi, S. Nakaya and N. Kajihara. *SOP: A reconfigurable massively parallel System and its Control-Data-Flow based compiling Method*. In Proceedings of Symposium on FPGAs for Custom Computing Machines, pages 148–156. IEEE, 1996. 33
- [Zhang 2003] X. Zhang, G. Dragffy, A. Pipe, N. Gunton and Q. Zhu. *A reconfigurable self-healing embryonic Cell Architecture*. In In Proceedings of the International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA), volume 1, page 4. Citeseer, 2003. 116
- [Zöllner 2012] M. Zöllner. *Modellierung von Parallelisierungsstrukturen für sequenzielle Algorithmen in C*. Bachelor Thesis, TU Darmstadt, January 2012. 127

[Zöllner 2014] M. Zöllner. *Parallelisierungstechniken für sequentiellen Code*. Final Thesis, TU Darsmtadt, February 2014. 137