Index

A
Adaptable Program Current Control Scheme (APCCS), 231–234, 243
Adaptable Slope Pulse Control (ASPC), 201–204, 207
Additional mask, 181, 182, 184, 194, 196, 206
Add-on flash, 22
Advanced Driver Assistance System (ADAS), 2, 3
Affinity with logic CMOS process, 42
Array architecture, 153
Array sector, 155
Automotive, 7, 12, 13, 16–19, 21, 25, 26, 75–77, 80, 81, 111, 113, 114, 117, 119, 122, 127, 128, 148, 179, 180, 182, 186, 201, 204, 207

B
Band-to-Band Tunneling (BTBT), 213, 215, 221
Band-to-Band Tunneling (BTBT) hot hole injection, 44–46
BCD, 148
Bluetooth®, 1
Breakdown voltage, 55, 57, 70
Byte (B), 22

C
Chanel Hot Electron (CHE) injection, 35
Channel FN electron ejection, 35, 40, 43
Channel FN hole injection, 44
Charge mismatch, 45, 46
Charge Pump (CP), 54, 55, 57, 84, 87, 91, 94–97, 101, 102, 104, 110, 113, 114, 116, 125, 223, 235–238
Charge-trapping, 179, 180, 211, 242, 243
Charge-Trapping(CT) structures, 31
Code flash, 8, 9, 12, 147
Code macro, 215, 217, 228
Code memory, 112, 113, 122, 127
Current sense, 190

D
Data flash, 12, 22, 26, 147
Data macro, 217
Data memory, 112, 113, 118, 120, 122, 127
Data retention, 148
2.5D/3D integration, 2
Defect, 35, 39, 42, 44–46, 48
Deplete, 179, 188, 192
DFM/DFT, 61, 62, 70
Digital-Signal Processor (DSP), 15
Disturb, 88, 89, 91, 113, 122, 123, 125, 126, 165
Drain/Source (D/S), 141
DRAM, 3

E
eFlash innovation, 3
eFlash macro, 13
eFlash MCU, 81
eFlash selection, 238
eFlash system, 29, 52, 62, 65–70
Electrically Erasable Programmable Read Only Memory (EEPROM), 7, 12, 20, 31, 49, 75, 82, 83, 111–113, 118, 120, 121, 131
Embedded flash, 147
Embedded flash memory (eFlash), 3–5, 91, 111, 180–182, 184, 204–207
Embeddedness, 3, 8
Embedded SuperFlash Gen 1 (ESF1), 133
Embedded SuperFlash Gen 2 (ESF2), 133
Embedded SuperFlash Gen 3 (ESF3), 133
Embedded system, 1–3
Endurance, 148, 180, 203, 204, 215, 233, 235, 241–243
Endurance (program/erase cycle), 29, 39
Erase unit/block, 36, 37, 52, 53

© Springer International Publishing AG 2018

H. Hidaka (ed.), *Embedded Flash Memory for Embedded Systems: Technology, Design for Sub-systems, and Innovations*, Integrated Circuits and Systems,
DOI 10.1007/978-3-319-55306-1

Error Correction Code (ECC), 62, 66–68, 151

F
FDSOI, 148
Field-Programmable Gate Array (FPGA), 15
Flash-MCU, 3, 209, 215, 224, 228, 235, 237
Floating Gate (FG), 179, 181, 183, 206
Floating Gate (FG) structures, 31
FN electron injection, 35, 36, 39–41, 43, 44, 46, 48, 49, 51
FN tunneling, 182, 187, 193, 194

H
Hierarchical architecture, 217
High performance, 209
High reliability, 209, 228, 233, 240, 243
HV circuit design, 52, 54, 55, 57, 70
HV decoder, 160
HV management, 76, 99
HV transistor, 77–79

I
Idling P/E Management Unit (IPEMU), 205, 206
Info rows, 156
Innovation, 7, 10, 11, 24–27
Integrated Device Manufacturer (IDM), 133
Intelligent Erase Scheme (IES), 233, 234, 243
Intelligent Slope Pulse Control Circuit (ISPCC), 201, 202
Internet of Everything (IoE), 1–3
Internet of Things (IoT), 2, 3, 147
IP, 17, 22

L
Level shift circuit, 56
Lightly Doped Drain (LDD), 77
Low cost, 179, 180, 184, 197, 206
Low power, 180–182, 203, 204
Low power design, 62

M
Macro, 21, 22
Macrocell, 76, 79, 90, 91, 98–100, 102, 106, 111, 122
Magnetic-RAM, 3
Mask ROM, 9, 10
MCU, 180, 181, 204, 206
Memory array, 32, 52, 54, 57, 58, 60, 65, 66, 70
Memory Gate (MG), 214
Metal-Oxide-Metal (MOM) capacitors, 236, 237
Metal-Oxide-Nitride-Oxide-Silicon (MONOS), 47, 48, 71
MG decoder, 194, 195–200
Micro-Controller Unit (MCU), 1, 3, 75, 76, 80–85, 89, 90, 94–96, 98, 99, 102, 103, 111, 117, 119, 120, 122, 126, 128
Multiple-Time Programmable (MTP) memory, 31

N
NAND-flash, 3
Nano-crystal/Nano-dot, 42, 43, 47, 48
Nitride film (Si_3N_4), 209–211, 224, 225, 243
Nominal VDD (Vddnom), 166
Non-boosted, 219
Non-volatility, 3
NOR, 75, 77, 85, 87, 118

O
One-Time Programmable (OTP) memory, 7–9, 30
Optical Process Correction (OPC), 158
Over-erase, 36–38, 40, 41, 46, 48
Oxide-Nitride-Oxide (ONO) film, 214
Oxide-RAM, 3

P
Page flash, 87
Poly-Insulator-Poly (PIP) capacitors, 236, 237
Poly to poly FN electron ejection, 36, 40
Pre-write, 192, 193
Program disturb, 37, 38, 53, 60, 185, 196, 215
Programmability, 3

R
RAM, 7, 21, 23
Random access, 228–230
Read circuit design, 52
Read disturb, 32, 46, 182, 185, 187, 188, 190, 196, 200
Read disturb free, 188, 189
Read Only Memory (ROM), 7–10, 12, 15, 18, 20, 21, 23, 131
Real-time, 1–3
Redundancy, 156
Reliability, 29–32, 38, 39, 41, 42, 45, 46, 52, 53, 60, 62, 65, 67, 70, 165, 179–181, 201, 206
Retention, 35, 39, 45, 46, 59, 209, 224–226, 241, 242

S
Safety function, 62, 66, 67, 71

Scalability, 36, 39, 42, 45
Sector erase, 85, 88
Secure, 75, 80–85, 89, 90, 94–96, 98, 99, 102, 120
Secure-MCU, 3, 20
Security, 11, 13, 15–18, 20–22, 25, 147
Security function, 49, 62, 66, 68
Sense amplifier, 217, 219, 227, 228, 243
Sense Amplifier with Digital Offset Cancellation (SA-DOC), 227, 228, 231, 243
Sensing, 161
Sensing scheme, 59, 60
SG-MONOS, 214, 223, 225, 240, 243
Simple structure, 181, 206
Smart card, 20, 150
Smart Clock Generator (SCG), 201–203
SONOS, 23, 42, 46, 48, 71, 179–181, 183, 185, 190
SONOS split-gate, 209–212, 214, 217–219, 221–225, 227, 231, 238, 240–243
Source FN electron ejection, 36
Source-Side Channel Hot Electron (SS CHE), 141
Source Side Injection (SSI), 35, 40, 44, 45, 71, 211, 213, 215, 221, 242
Split-gate, 148
Split-gate cell structure (1.5Tr), 32, 33, 35, 37, 40, 41, 47, 48, 58
Spread Spectrum Clock Generation (SSCG), 237, 238, 243
SRAM, 3
Standard IO-MOS, 195–200
Stress Induced Leakage Current (SILC), 39–41, 45, 140
SuperFlash, 148

T
1T, 111–113, 115–117, 119, 120, 122, 123
TDDB, 229, 240
Thermionic emission, 224, 225
Threshold voltage (Vt), 164
1.5Tr, 209, 211
1 Transistor cell structure (1Tr), 31–33, 36, 37, 40, 41, 46, 48, 51–53, 58, 71
2 Transistor cell structure (2Tr), 32, 33, 37, 40, 41, 48, 50, 58, 71
Trap distribution, 225, 226
1Tr-SONOS, 179–187, 189, 190, 194, 195, 198, 204–207
1Tr. structure, 179, 180, 187, 192

V
Voltage switch (VSW), 54

W
Word Line (WL), 209, 219, 240

X
X-Decoder (XDEC), 158