Appendix A
List of Symbols

Symbols	Explanation
1 dB	1 Decibel
2-D	Two dimensional
3-D	Three dimensional
A	Gate area
AC	Alternating current
C_{bd}	Bulk-drain junction capacitance
C_{bs}	Bulk-source junction capacitance
C_{ds}	Drain-source capacitance
C_{DG}	Capacitance of DG MOSFET
C_{dSi}	Drain to source intrinsic capacitance
C_G	Gate capacitance
C_{gb}	Gate to bulk capacitance
C_{gd}	Gate to drain capacitance
C_{gs}	Gate to source capacitance
C_{in}	Input capacitance
CMOS	Complementary metal oxide semiconductor
C_{out}	Output capacitance
C_p	Capacitance value measured with parallel equivalent circuit model
C_s	Capacitance value measured with series equivalent circuit model
DC	Direct current
DIBL	Drain-induced barrier lowering (short channel effect)
DUT	Device under test
E_C	Conduction band
E_g	Band gap of silicon, 1.12 ev at 300 K
ESD	Electrostatic discharge
FD	Fully depleted
FET	Field effect transistor
F_{max}	Maximum frequency of oscillation
f_T	Cross-over frequency
GaAs	Gallium arsenide
GHz	Gigahertz

(continued)

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(continued)

Symbols	Explanation
HBM	Human body model
IC	Integrated circuit
I_d	Drain current
I_{dc}	Direct current electricity
I_{ds}	Drain to source current
IF	Intermediate frequency
IL	Insertion loss
ILD	Inter layer dielectric
ISO	Isolation loss
k	Boltzmann constant
L	Channel length
LNA	Low noise amplifier
MEMS	Micro electro mechanical system
MESFET	Metal Semiconductor Field Effect Transistor
MMIC	Monolithic microwave integrated circuit
MOS	Metal oxide semiconductor
MOSFET	Metal oxide semiconductor field effect transistor
n	Concentration (density) of free electrons
N_A	Channel doping concentration of acceptors
$N_{D/S}$	Source/drain doping concentration
NF	Number of parallel devices in a multi-finger layout
n_i	Intrinsic electron density in silicon, 1.45×10^{10} cm^{-3} at 300 K
nm	Nanometer
NMOS	N type MOS transistor
NQS	Non-quasi-static
PA	Power amplifier
PD	Partially depleted
PIN	P-type-Intrinsic-N-type
q	Electron charge
$q/(kT)$	38.68 V^{-1} at 300 K
Q_B	Bulk charge
Q_{BD}	Bulk to drain junction charge
Q_{BS}	Bulk to source junction charge
Q_D	Drain charge
Q_{GB}	Gate to bulk charge
Q_I	Inversion charge
Q_{inv}	Inversion carrier sheet density
Q_S	Source charge
Q_{TH}	Inversion carrier sheet density under threshold conditions
R	Resistance
R_b	Bulk resistance
R_{bd}	Substrate resistance between substrate drain node and bulk node
R_{bs}	Substrate resistance between substrate source node and bulk node
R_d	Drain resistance
R_{dc}	Direct current resistance
R_{DG}	Resistance of DG MOSFET

(continued)

(continued)

Symbols	Explanation
R_{ds}	Parasitic drain to source resistance in parallel with the MOS channel
R_{dsb}	Substrate resistance between internal bulk node and substrate node
RF	Radio frequency
RFC	Radio frequency chokes
R_g	Gate resistance
R_{in}	Input resistance
R_{out}	Output resistance
R_p	Equivalent parallel resistance measured with parallel equivalent circuit model
R_s	Equivalent series resistance measured with series equivalent circuit model
s	Laplace term
S	Scattering parameters
SAW	Surface acoustic wave
SOI	Silicon on insulator
SOS	Silicon on sapphire
T	Absolute temperature
T/R	Transmit/receive
t_I	Thickness of the gate dielectric (insulator) layer
t_{ox}	Thickness of the gate oxide layer
t_{Si}	Thickness of silicon film (channel)
V_{bd}	Body to drain voltage
VCO	Voltage-controlled oscillator
V_{dc}	Direct current voltage
V_{dg}	Drain to gate voltage
V_{ds}	Drain to source voltage
$V_{F,eff}$	Effective front gate voltage
Vgs	Gate to source voltage
$V_{gs,B}$	Bottom (back) gate voltage
$V_{gs,F}$	Front gate voltage
V_H	Higher effective gate voltage
V_{in}	Input voltage
V_L	Lower effective gate voltage
V_{out}	Output voltage
V_{th}	Threshold voltage
V_T	Thermal voltage
W	Channel width
WLAN	Wireless local area networks
X	Reactance
Y	Admittance
Z	Impedance
Z_0	Reference impedance level (50 Ω in this book)
Z_{in}	Input impedance
Z_{out}	Output impedance
ε_0	Dielectric constant of vacuum, $8.854*10^{-12}$ Fm^{-1}
ε_I	Permittivity (relative dielectric constant) of gate dielectric (insulator)

(continued)

(continued)

Symbols	Explanation
ε_{Si}	Permittivity (relative dielectric constant) of silicon, 11.9
ε_{SiO2}	Relative dielectric constant of silicon dioxide (SiO_2), 3.9
λ_{Di}	Intrinsic Debye length, 48.49 μm at 300 K
φ_F	Potential difference between Fermi level and quasi-Fermi level
Φ_i	Work function of intrinsic silicon, 4.71 ev at 300 K
Φ_M	Work function of gate material
Φ_{MB}	Work function of bottom (back) gate material
Φ_{MF}	Work function of front gate material
Φ_{MS}	Work function difference between gate material and doped silicon
$\Phi_{MS,i}$	Work function difference between gate material and intrinsic silicon
ω	Angular frequency
ΔS_{11m}	Measurement error of S_{11} magnitude
ΔS_{12m}	Measurement error of S_{12} magnitude
ΔS_{21m}	Measurement error of S_{21} magnitude
ΔS_{22m}	Measurement error of S_{22} magnitude
μm	Micrometer

Appendix B
List of Definitions

1 dB compression point	The 1 dB gain compression point is the input power level in dBm at which the overall gain of amplifier is reduced by 1 dB from its maximum value
Design for manufacturability (DFM)	Design and verification methodology employed to assure that production silicon yields a suitable percentage of die, meeting the design specifications
Design for performance (DFP)	Design and verification methodology employed to assure that production silicon meets the performance objectives of the original circuit design
Design for reliability (DFR)	Design and verification methodology employed to assure that the IC performance does not substantially degrade over the anticipated lifetime of the product
Design rule check (DRC)	A check of physical layout using a foundry-determined set of rules or more complex computations to include the effect of nearby lithographic patterns
Design rules	Design rules are constraints poses by the processing line in the form of minimum allowable values for width, separation, extension and overlap. The complexity of design rules depends upon how well a process is characterized

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Doped semiconductor	To improve the conductivity, impurities are added in intrinsic (pure) semiconductors. To increase the number of electrons Arsenic or Phosphorous is added into Si. It has five electrons in its outer shell. Four of these five electrons bond with adjacent silicon atoms, but the fifth electron cannot form a bond
Drain-induced barrier lowering (DIBL)	The effect of drain field reaching through the channel and lowering the source-channel energy barrier, thereby resulting in reductions in threshold and increases in output conductance with drain voltage
Fabrication steps	These steps are Wafer processing, Mask making, Photolithography, Oxidation, Diffusion, Etching, Poly-gate formation, and Metallization
Figure-of-merit (FOM)	A normalized quantity calculated based on several analog circuit performance parameters that enable a comparison of the quality of circuits having different performance parameters
Finite difference method (FDM)	The FDM subdivides the simulation domain into small discrete segments separated by nodal points. The method is based on defining unknown variable only on these nodal points assuming linear variation in between
Gain-bandwidth product (GBW)	Gain-bandwidth is defined simply as gm = Cox and is used here for the purpose of determining how GBW varies, rather than a numerical value
High dielectric constant (High-K)	Term used in nanoscale technology nodes referring to gate materials that have higher dielectric constants than oxynitrde, such as hafnium and zirconium
Hot carrier injection (HCI)	Carrier injection into the channel or gate insulator produced by impact ionization near the drain end of the channel creating interface and oxide trap damage
Low dielectric-constant material	The material having lower dielectric constant than the SiO_2 used prior to nanoscale technology nodes
Low-power process (LP) device	Low-power incorporate thicker oxides than the high-performance to reduce logic power using higher thresholds and lower leakages. LP have higher saturation voltages, lower transconductance, higher output conductance, and significantly lower gain-bandwidths

Maximum excess overdrive supply voltage ($V_{CC,EOD}$)	The maximum drain-to-source voltage for devices with drain voltage waveforms that allow safe operation at voltages above $V_{CC,OD}$
Maximum overdrive supply voltage ($V_{CC,OD}$)	The maximum drain-to-source voltage for core devices that are not operated at high drive currents
Maximum supply voltage ($V_{CC,MAX}$)	The maximum gates to source drain to source, or source to bulk voltage for simulation purposes
Metal–insulator–metal capacitor (MIM)	It is a technology using a thin insulator between intermediate interconnect metal and an added metal to create a precise capacitor in an analog process
Minimum-gate-length feature size	Minimum gate feature size in the physical layout
Negative bias temperature instability (NBTI)	Threshold voltage instability in p-MOS devices that is dependent on temperature and device geometry
Overdrive (OD)	An operating condition permitted by design rules where some devices, such as core devices, may exceed normal operating parameters such as voltages
Power amplifier (PA)	A power amplifier is a component of transmitter frontend, used to amplify the RF signal to very high levels for transmission from the external antenna
Scaling of device	It refers to ordered reduction in dimensions of the MOSFET and other VLSI features. It allows the same decision to be made using less power and area and thus drives the electronic revolution
System-on-chip (SOC)	Technology that enables integration of all necessary electronic circuits for a complete system on a single integrated circuit
Technology based computer-aided design (TCAD)	It is used to define the physical configuration of devices within the silicon and then determines device (or simple circuit) performance using physical models of carrier propagation
Threshold voltage	The voltage on gate required to create inversion layer is called threshold voltage

Appendix C
Outcomes of the Book

1. Each gate controls one half of the device and its operation is completely independent of the other
2. Two independent MOSFETs on a single chip whose operations are independent of the other
3. Board component count and hence total cost decreases
4. The total current through the device should be the sum of the currents through the separate devices
5. The performance of the symmetrical version of the DG MOSFET is further increased by higher channel mobility compared to a bulk MOSFET
6. The average electric field in the channel is lower, which reduces interface roughness scattering according to the universal mobility model
7. One of the major advantages of using DG MOSFET is the lower leakage current and smaller subthreshold voltage
8. For single gate MOSFET, at ON condition of a transistor, increasing C_{sb} and C_{db} tends to more signal being coupled with the substrate and dissipated in the substrate resistance (R_b), so the design would like that no signal being coupled with the substrate and dissipated in the substrate resistance
9. The isolation is better in DG MOSFET compared to that in the single-gate MOSFET in terms of drain-to-source capacitance ($C_{DG} > C_{SG}$)
10. ON-state resistance is low, which shows that the current flows from source-to-drain in a MOSFET ($R_{DG} < R_{SG}$)
11. For appropriate working of a switch and to reduce the insertion loss, we have achieved the reduction in ON-state resistance with selecting transistor with large μ, increasing W/L, keeping $V_{gs} - V_{th}$ large
12. Bulk capacitors are not taken into account for the design
13. Highest drain current can be easily achieved by using the higher number of fingers
14. Reduction in the threshold voltage occurs due to the random dopant fluctuations (by the use of intrinsic or lightly doped body, in the DG MOSFET)

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15. Due to the single operating frequency, SPDT type of switch has a limited data transfer rate. Therefore, a Double-Pole Double-Throw (DPDT) switch is designed to solve the problem
16. The DPDT switch has dual antenna and dual ports, one port for transmitting and the other for receiving, which is not sufficient for MIMO systems. Hence, we design a DP4T switch to enhance the switch performance for MIMO applications
17. A traditional DP4T n-MOS switch uses n-MOS as transistors in its main architecture and requires a control voltage of 5.0 V, while the proposed device has low control voltage
18. The switch is designed to be part of the microwave applications for switching system between the transmitting and receiving modes
19. The isolation of switch is improved by grounding RF signals on the side which is turned OFF
20. With scaling device dimensions and increasing short channel effects, multiple gate transistors can be investigated to obtain an improved gate control
21. Achieving high isolation in the OFF-state and low insertion loss in the ON-state for wideband applications is quite a challenge for switch designers
22. The channel resistance of a switch must be limited to less than about 6 Ω to achieve a low frequency insertion loss of less than 0.5 dB on a line with 50 Ω matched impedances at the source and load
23. More than 50 % of footprint saving are achieved as compared to two single-gate MOFETs, less pick and place effort
24. Energy stored is greater than 1.4 times for CSDG MOSFET compared to CSSG MOSFET
25. Replacement of traditional SiO_2 gate dielectrics with HfO_2 is mainly for requirement of high-k dielectrics
26. To improve the integration and performance of CMOS devices, and its applications, Hf-based gate layers are being integrated into DG MOSFET to achieve low leakage current
27. Excellent gate transistors with improved performance based on Hf-based gate dielectrics as the insulating layers are achieved
28. For the purpose of RF switch, we have achieved the process to minimize control voltage and minimization of the resistance for the switch-ON condition
29. Since the HfO_2 has melting point 2,812 °C, the designed DP4T switch can work sufficiently for high-power switches, Jacket water temperature, and process temperature and also for broadband and carbon nanotube-based nonvolatile RAM
30. Image acquisitions are used to observe the edges of the rectangular and cylindrical devices
31. The proposed model emphasized on the basics of the single image sensor for two-dimensional images of three-dimensional devices
32. Using image acquisitions technique, we can verify the basics of the circuit elements parameter required for the radio frequency subsystems of the integrated circuits

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