Appendix 1

In chapter 4, a formula has been derived that accurately predicts the relationship between the mismatch behaviour of the current source transistors and the achievable INL.yield of the current steering D/A converter. This formula is given by:

\[
\frac{\sigma(I)}{I} = \frac{1}{2\sqrt{2^N C}}
\]

(1)

with \( C = \text{inv.norm}_{(-x,x)}(0.5 + \frac{\text{INL.yield}}{2}) = \text{inv.norm}_{(-x,x)}(z) \).

In fig.1, the value for C can be found starting from the specification for the INL.yield or starting from the calculated value for z. From the same figure, it is also possible to obtain the value for C starting from the allowed percentage of faults that can be tolerated.
<table>
<thead>
<tr>
<th>$z$</th>
<th>inv norm($z$)</th>
<th>Yield [%]</th>
<th>Faults [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.50000</td>
<td>0.00</td>
<td>0.00</td>
<td>100.00</td>
</tr>
<tr>
<td>0.57926</td>
<td>0.20</td>
<td>15.85</td>
<td>84.15</td>
</tr>
<tr>
<td>0.65542</td>
<td>0.40</td>
<td>31.08</td>
<td>68.92</td>
</tr>
<tr>
<td>0.72575</td>
<td>0.60</td>
<td>45.15</td>
<td>54.85</td>
</tr>
<tr>
<td>0.78814</td>
<td>0.80</td>
<td>57.63</td>
<td>42.37</td>
</tr>
<tr>
<td>0.84134</td>
<td>1.00</td>
<td>68.27</td>
<td>31.73</td>
</tr>
<tr>
<td>0.88493</td>
<td>1.20</td>
<td>76.99</td>
<td>23.01</td>
</tr>
<tr>
<td>0.91924</td>
<td>1.40</td>
<td>83.85</td>
<td>16.15</td>
</tr>
<tr>
<td>0.94520</td>
<td>1.60</td>
<td>89.04</td>
<td>10.96</td>
</tr>
<tr>
<td>0.96407</td>
<td>1.80</td>
<td>92.81</td>
<td>7.19</td>
</tr>
<tr>
<td>0.97725</td>
<td>2.00</td>
<td>95.45</td>
<td>4.55</td>
</tr>
<tr>
<td>0.98610</td>
<td>2.20</td>
<td>97.22</td>
<td>2.78</td>
</tr>
<tr>
<td>0.99180</td>
<td>2.40</td>
<td>98.36</td>
<td>1.64</td>
</tr>
<tr>
<td>0.99534</td>
<td>2.60</td>
<td>99.07</td>
<td>0.93</td>
</tr>
<tr>
<td>0.99744</td>
<td>2.80</td>
<td>99.49</td>
<td>0.51</td>
</tr>
<tr>
<td>0.99865</td>
<td>3.00</td>
<td>99.73</td>
<td>0.27</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.99931286</td>
<td>3.20</td>
<td>99.862572</td>
<td>1.37E-01</td>
</tr>
<tr>
<td>0.99966307</td>
<td>3.40</td>
<td>99.932614</td>
<td>6.74E-02</td>
</tr>
<tr>
<td>0.99984089</td>
<td>3.60</td>
<td>99.968178</td>
<td>3.18E-02</td>
</tr>
<tr>
<td>0.99992765</td>
<td>3.80</td>
<td>99.985530</td>
<td>1.45E-02</td>
</tr>
<tr>
<td>0.99996833</td>
<td>4.00</td>
<td>99.993666</td>
<td>6.33E-03</td>
</tr>
<tr>
<td>0.99998665</td>
<td>4.20</td>
<td>99.997331</td>
<td>2.67E-03</td>
</tr>
<tr>
<td>0.99999459</td>
<td>4.40</td>
<td>99.998917</td>
<td>1.08E-03</td>
</tr>
<tr>
<td>0.99999789</td>
<td>4.60</td>
<td>99.999578</td>
<td>4.22E-04</td>
</tr>
<tr>
<td>0.99999921</td>
<td>4.80</td>
<td>99.999943</td>
<td>1.59E-04</td>
</tr>
<tr>
<td>0.99999971</td>
<td>5.00</td>
<td>99.999943</td>
<td>5.73E-05</td>
</tr>
<tr>
<td>0.99999990</td>
<td>5.20</td>
<td>99.999980</td>
<td>1.99E-05</td>
</tr>
<tr>
<td>0.99999997</td>
<td>5.40</td>
<td>99.999993</td>
<td>6.66E-06</td>
</tr>
<tr>
<td>0.99999999</td>
<td>5.60</td>
<td>99.999998</td>
<td>2.14E-06</td>
</tr>
<tr>
<td>1.00000000</td>
<td>5.80</td>
<td>99.999999</td>
<td>6.63E-07</td>
</tr>
<tr>
<td>1.00000000</td>
<td>6.00</td>
<td>100.000000</td>
<td>1.97E-07</td>
</tr>
</tbody>
</table>

Figure 1: The value of the parameter $C$ as a function of the INL yield
Appendix 2

In this appendix, the complete derivation of the SFDR as a function of the second and third order harmonic distortion is given. The main results were given in chapter 5.

For a \( \sin(\omega t) \) output signal, the number of switches \( T \) that conduct current at a time \( t \) equals:

\[
T(t) = S \left( \frac{1 + \sin(\omega t)}{2} \right)
\]  \hspace{1cm} (1)

with \( S \) the total number of current sources.

The output voltage of the D/A converter is determined by the product of the current and the load impedance \( Z_L \) in parallel with \( T(t) \) parallel impedances \( Z_{imp} \):

\[
V_{out}(t) = \frac{SI(1 + \sin(\omega t))}{2Y_L + Y_{imp}S(1 + \sin(\omega t))}
\]  \hspace{1cm} (2)

with \( I \) the current through one switch transistor and \( Y_{imp} = 1/Z_{imp} \) and \( Y_L = 1/Z_L \). A Taylor series expansion of the output voltage allows to determine the influence of \( Y_{imp} \) on the dynamic performance of the D/A converter.

\[
V_{out}(t) = (DC)_{cf} + A\sin(\omega t) + B\sin^2(\omega t) + C\sin^3(\omega t) + D\sin^4(\omega t) + \ldots
\]  \hspace{1cm} (3)
Applying goniometric relations and rearranging of the terms leads to the following result:

\[ V_{out}(t) = (DC)_{cf} + \left[ A + \frac{3C}{4} \right] \sin(\omega t) + \left[ \frac{-(B + D)}{2} \right] \cos(2\omega t) \]

\[ - \left[ \frac{C}{4} + \frac{5E}{16} \right] \sin(3\omega t) + \left[ \frac{D}{8} + \frac{3F}{16} \right] \cos(4\omega t) \ldots \]  

Inserting the values of eq.4 in eq.5 in order to determine the influence of the second order harmonic on the SFDR performance of a current steering D/A converter, yields the following result:

\[ Q = \frac{1}{4} \frac{(2Y_L + SY_{imp})(16Y_L^2 + 16SY_LY_{imp} + 7S^2Y_{imp}^2)}{SY_{imp}(2Y_L^2 + 2SY_LY_{imp} + S^2Y_{imp}^2)} \]  

The influence of the third order harmonic is described by:

\[ T = -4 \frac{(2Y_L + SY_{imp})^2(16Y_L^2 + 16SY_LY_{imp} + 7S^2Y_{imp}^2)}{S^2Y_{imp}^2(16Y_L^2 + 16SY_LY_{imp} - 9S^2Y_{imp}^2)} \]  

Since \( Y_L \gg SY_{imp} \), both equations can be further simplified to:

\[ Q = \frac{4Y_L + 2SY_{imp}}{SY_{imp}} \approx \frac{4Y_L}{SY_{imp}} \]
and
\[ T = \left( \frac{4Y_L + 2SY_{imp}}{SY_{imp}} \right)^2 \approx \left( \frac{4Y_L}{SY_{imp}} \right)^2 \] (9)

or written in function of the SFDR:
\[ HD2 = 20 \log(Q) = 20 \log\left( \frac{4Z_{imp}}{SZ_L} \right) \] (10)

and
\[ HD3 = 20 \log(T) = 20 \log\left( \frac{4Z_{imp}}{SZ_L} \right)^2 \] (11)

From this derivation, it becomes clear that if for a 10 bit D/A converter the HD2 distortion component equals 60 dB, the HD3 distortion component equals 120 dB. It can therefore be concluded that the influence of the frequency dependency of the output impedance has a negligible effect on the third order harmonic distortion component.
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