Summary

This thesis describes the theory, design and realization of precision interface electronics for bridge transducers and thermocouples that require high accuracy, low noise, low drift and simultaneously, low power consumption. This thesis is dedicated to two aspects: (1) the design of precision stand-alone instrumentation amplifiers (IAs) that can be used to drive an external Analog-to-Digital Converter (ADC); (2) the design of a read-out IC that combines an instrumentation amplifier and an ADC. Several new concepts and techniques have been proposed and verified in CMOS technology.

Chapter 1

An introduction and motivation of the work described in this thesis is given in this chapter. Precision bridge transducers and thermocouples typically output low-frequency (LF) signals of a few Hz with millivolt levels. Therefore, they require instrumentation amplifiers (IAs) with input-referred errors at the microvolt- or nanovolt- level to boost such signals to levels compatible with the typical input ranges of subsequent analog-to-digital converters (ADCs). Since sensor output signals are often either ground-referenced or accompanied by a large common-mode (CM) voltage, such IAs require ground-sensing capability and a high common-mode rejection ratio (CMRR) (>120 dB).

Current-feedback Instrumentation amplifiers (CFIAs) are well-suited for bridge read-out because of their high CMRR, ability to handle different input and output CM voltages and power efficiency. However, their main disadvantages are limited gain accuracy due to the mismatch of the input and feedback transconductors and limited input range due to the non-linearity of these transconductors. This thesis focuses on the design of improved CFIAs.

Furthermore, the CFIA can be used as a preamplifier and combined with an ADC to comprise a read-out IC. For instrumentation applications, the incremental

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ΔΣ ADCs are very suitable. The IAs in previous read-out ICs generally employed switched-capacitor (SC) or two-opamp IA topologies. Neither of these topologies is particularly power efficient. Since CFIAs are more power efficient, this thesis presents the design of a read-out IC that combines a CFIA and an ADC, both of which collaborate to achieve an optimum performance.

As a test-case, the challenging task of developing interface electronics for a precision thermistor bridge is described. This is intended for use in wafer steppers where μK-level temperature resolution is required. The resulting interface electronics is also applicable to other sensors, e.g. strain gauges, thermocouples and Hall sensors.

Chapter 2

Chapter 2 gives an overview of dynamic offset cancellation techniques such as chopping, auto-zeroing and offset-stabilization. It also shows how to apply these techniques to operational amplifiers. It is shown that since chopping is a continuous-time modulation technique that does not cause noise folding and is thus superior than auto-zeroing. However, in stand-alone amplifiers, the modulated $1/f$ noise and offset need to be suppressed to ensure a ripple free output.

There are numerous ways to eliminate chopper ripple, such as auto-zeroing, switched-capacitor (SC) or continuous-time (CT) notch filters or the use of an auto-correction feedback loop. The SC sampling techniques incur a certain noise folding penalty. The CT notch filter requires a good matching between the period of the chopping clock and the notch position in the CT filter. Furthermore, all the above-mentioned techniques suffer from the excess phase shift introduced by the notch filter. Therefore, a high chopping frequency (or a low unity-gain-bandwidth of the amplifier) is required to maintain stability. A new ripple reduction technique is proposed in Chap. 4 that avoids all these issues.

Chapter 3

The use of dynamic offset compensation techniques is extended to precision CFIAs, since they are well suited for bridge read-out. However, the gain accuracy of a CFIA is rather limited due to the mismatch between its input and feedback transconductors. Several techniques can be applied to improve its gain accuracy, such as resistor-degeneration, auto-gain calibration and dynamic element matching (DEM). However, resistor-degeneration requires significantly more power and auto-gain calibration can not maintain a continuous output signal. DEM improves gain accuracy by modulating the G_m mismatch to the DEM frequency, thus giving rise to a signal dependent ripple. To eliminate the DEM ripple, trimming can be used. However, it increases production costs and will not compensate for temperature drift. A new technique is proposed in Chap. 5 that eliminates the need of trimming.

Chapter 4

The architectural design and implementation of a stand-alone chopper CFIA are described. It consists of three gain stages, in which the input and intermediate stages are both chopped at 30 kHz to suppress their 1/*f* noise and also to provide sufficient gain to suppress the 1/*f* noise of the unchopped output stage. To suppress the chopper ripple due to the offset of the input stage, a continuous-time offset reduction loop (ORL) is proposed, while the chopper ripple associated with the intermediate stage was suppressed by chopping it at a much higher frequency (510 kHz).

The ORL uses a synchronous detection technique to demodulate the ripple, and then drives the ripple to zero by continuously compensating for the offset. Due to its continuous-time nature, the ORL does not cause noise folding. Furthermore, the ORL is inherently stable, which is the key advantage compared to other ripple reduction techniques using notch filters or auto-correction feedback loop. A low chopping frequency can thus be chosen for low offset. Other authors have shown that the ORL can also be applied to general-purpose chopper CFIAs and operational amplifiers.

Measurement results show that the ORL reduces the amplitude of the chopper ripple by a factor of 1100, to levels below the amplifier's own input-referred noise level. The CFIA achieves 1 mHz 1/*f* noise corner at a noise PSD of 15 nV/$\sqrt{\text{Hz}}$ while consuming only 230 μA supply current (NEF = 8.8), which is quite respectable compared to previous work. To the authors' knowledge, this represents the best LF noise performance ever reported for a stand-alone CMOS instrumentation amplifier.

Chapter 5

The chopper CFIA described in the previous chapter achieves microvolt-level offset and a high CMRR (>120 dB). However, its gain error, mainly determined by the mismatch of the input and feedback transconductors (noted as "Δ"), is about 0.5 %, which becomes the dominant source of residual error. Thus, the design and implementation of a CFIA with improved gain accuracy are discussed in this chapter.

To improve gain accuracy, dynamic element matching (DEM) is applied to the input and feedback transconductors of the CFIA, so as to average out their mismatch. DEM modulates the G_m mismatch to the DEM frequency, thus giving rise to a signal-dependent ripple at CFIA output. To suppress this ripple, a gain error reduction loop (GERL) is proposed to continuously null the mismatch of the input and feedback transconductances, thus eliminating the need for trimming.

Unlike the ORL, which feeds back an additive offset-compensating signal, the GERL feeds back a *multiplicative* gain-compensating signal, which adjusts the

ratio of the input and feedback transconductances. The output DEM ripple is then the product of the mismatch and the output signal, and so the gain of the GERL will be signal dependent. To guarantee negative feedback, a polarity reversing switch is used to link the polarity of the GERL to that of the output signal.

The loop gain of the GERL is proportional to the input signal and so is zero for zero input. In this case, leakage causes the integrator output $V_{\text{int,GE}}$ to drift with a time constant of several seconds and eventually clip. The GERL will then need to resettle whenever a finite input signal re-appears. To avoid the need for resettling, a digitally-assisted GERL is implemented to store the mismatch information in the digital domain in this circumstance. For comparison, the analog implementation of the GERL is also implemented.

DEM reduces the gain error from Δ to $\Delta^2/2$, moving the average input and feedback transconductances closer to each other. This results in a CFIA with improved gain error, gain drift and linearity. The GERL improves matters further, since it drives the mismatch to zero. As a result, the average input and feedback transconductors become even more closely *aligned*. Finally, the use of DEM and the GERL also increases the linear input range of the CFIA by a factor of three.

Measurement results show that without trimming, the CFIA achieves a gain error of less than 0.06 % and a maximum gain drift of 6 ppm/°C in a power efficient manner (NEF = 11.2). Compared to a CFIA with similar gain accuracy, but using resistor-degenerated input stages, this represents a 4× improvement in power efficiency, which is equivalent to a 16× less power when achieving the same noise level. These measurement results confirm that the combination of DEM and the GERL is a power-efficient manner of improving the gain accuracy, gain drift and linearity of a CFIA.

Chapter 6

The CFIA described in Chap. 4 is then combined with a switched-capacitor sigma–delta ($\Delta\Sigma$) ADC to realize a read-out IC. The system-level design and implementation of the read-out IC are described. The CFIA provides high input impedance for bridge read-out and relaxes the noise and offset requirements of the ADC. The ADC employs a topology whose gain accuracy does not depend on component matching. Furthermore, the use of a ratio-metric topology means that the accuracy of the ADC's reference is much relaxed. These two solutions enable the ADC to achieve a gain error of less than 2 ppm. Thus, the gain error of the read-out IC is mainly determined by the mismatch between the input and feedback transconductors of the CFIA.

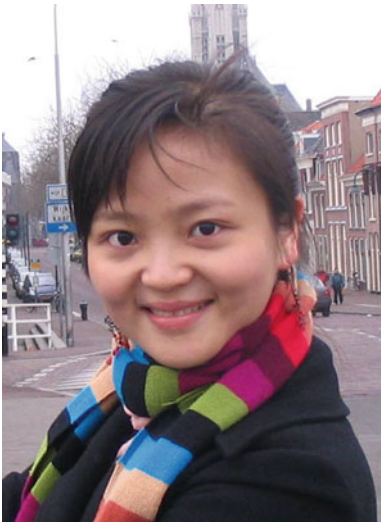
To eliminate this mismatch, DEM is applied to the two transconductors to average out their mismatch. However, the CM dependency of these transconductors limits the achievable gain accuracy even with DEM applied. To enhance their CM immunity, bulk-biasing and impedance-balancing techniques are employed. To reduce gain error and gain drift further, a digitally-assisted gain

error correction (GEC) scheme is applied, which digitally processes the output of the ADC and feeds back a gain error correcting signal. This improves the gain accuracy and gain drift of the CFIA. Overall, the GEC path serves as a coarse-trim of G_m mismatch, while the DEM acts as a fine-trim that compensates for temperature drift.

To reduce offset to the nV-level, system-level chopping is employed to chop the entire read-out chain during multiple conversions. The modulated offset is then averaged out in the decimation filter. It has been found that the combination of input stage chopping in the CFIA and system-level chopping is a better way to suppress 1/*f* noise and offset, compared to the use of multi-stage chopping. Measurement results show that the former achieves 0.1 mHz 1/*f* noise corner, while the latter achieves 1 mHz 1/*f* noise corner. Furthermore, in the former approach, the choppers in the intermediate stage of the CFIA are off, thus avoiding extra offset due to the coupling of charge injection and clock spikes through the Miller-compensation capacitor. The ultimate residual offset of the read-out IC is then determined by its resolution and is about 48 nV.

Measurement results show that the read-out IC achieves state-of-art 1/*f* noise corner (0.1 mHz), offset (48 nV), gain drift (1.2 ppm/°C), offset drift (6 nV/°C) and power efficiency (FOM = 111 pJ/Conv). These qualities make the proposed read-out IC very suitable for demanding bridge transducer applications, which require low thermal and 1/*f* noise, high accuracy, low drift, and simultaneously, low power consumption.

About the Author



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