The topics covered in this book deal with the interrelation between low-power and test of VLSI circuits. The reader has been introduced first to the basic concepts in manufacturing test and power issues during test. In order to avoid destructive testing and overkill, various solutions adopted to reduce power during test have been developed. In the first part of the book, the emphasis was placed on solutions for low-power ATPG, power-aware DFT, BIST and test data compression and power-conscious system-level test planning. The presence of power-management structures, such as clock gating, power gating or multiple supply voltages, introduces additional constraints on the testing process. Therefore, in the second part of the book, the focus was shifted toward the unique test requirements for low-power devices. The book concludes with an overview of the challenges faced by the EDA industry to integrate the constraints and objectives for designing low-power and testable VLSI circuits.

Over the past few decades, the consumers have benefited from Moore’s Law by gaining more functionality when shifting from one process node to the next one. As we have already seen in the past few years, the power wall has altered this trend, and innovations in technology, circuits and architectures are necessary to get the most out of the nano-scale process nodes and maintain their performance benefits and hence the added functionality over time. As final remarks for this book, we briefly look at three different directions pursued these days to manage the excessive power requirements and understand their implications on the test technology. These directions can be broadly classified as technology, circuit and architecture oriented.

On the integration technology side, there are major ongoing initiatives for implementing 3D integrated devices. Placing active devices on multiple tiers within the same package can reduce the power consumed by long interconnects and device pins. This, in turn, provides an opportunity to boost the performance without exceeding the power budgets constrained by heat density, packaging and cooling equipment. Nevertheless, regardless how 3D integration is achieved, i.e. through stacked chips, wafer-scale or monolithic integration (each of them with different fabrication cost and size for through-silicon vias), the test technology will need to keep up in order to test these devices cost-effectively. For example, interconnects between layers may require new fault models and devising thermal-aware test plans for 3D circuits will present unique challenges to the test technology.
Future process technologies will introduce even more design variability and predicting circuit performance will become more difficult as the feature size continues to decrease. A worst-case design approach will be impractical either due to performance or yield concerns. As a consequence, there has been a growing interest in using resilient circuits that can tolerate the process parameter variations, temperature gradients or fluctuations in supply voltages, all of which influence power. The use of on-chip temperature and voltage sensors, combined with self-adaptive circuits, has been shown to allow body bias, operating frequency and supply voltage to be dynamically adjusted. Similarly, error detection circuitry can be employed to detect timing errors at runtime, in which case additional clock cycles are required for rollback and recovery. This enables circuit operation at better than worst-case clock period; and as long as the timing errors are not frequent, the improvement in clock frequency outweighs the penalty in clock cycle count. There is little doubt that relaxing the focus from worst-case design will benefit power; however, new test challenges will arise. Screening the fabrication defects in logic blocks in the presence of resilient circuits is not a trivial task and these circuits will also need to be thoroughly characterized and tested for defects, as they are the infrastructure that enables self-adaptation in-field. Besides, guaranteeing their correct operation in-field will require a better understanding how online test and diagnosis can be done in a power-efficient way.

It is well known that multi-core processors are becoming the standard computing architecture. One of the major reasons for their adoption was the power wall faced by the single-core processors, which have relied primarily on scaling the operating frequency for a boost in performance. With the burden shifted to software development, on-chip parallel computing provided by multi-cores is enabling a further improvement in performance. As we gradually move from two to quad to eight and so on to “hundreds-of-core” processors, some of these cores will be used to improve yield and reliability by means of fault tolerance for permanent faults and self-adaptation for transient errors. As it was the case with resilient circuits, the self-adaptive architectural features, which decide at runtime the load on each processor, will pose unique challenges to the test technology. An example is the creation of power-constrained test plans that take into account the temperature gradients for validating the self-adaptive architectural features. On another line of thought, multi-core architectures will provide the opportunity to rethink some of the fundamental EDA algorithms, including ATPG, DFT insertion, test data compression and so on; most of these algorithms will deal with power constraints and hence multi-core architectures will enable a faster and better implementation.

Low-power testing is an active area of research and development that has steadily moved from research labs to practice in the past decade. This book has detailed both the basic and the advanced techniques in the field. It is anticipated that with the growing need for more power efficiency, the low-power testing techniques presented in this book will continue to be widely adopted. With the ongoing advances in technology, circuits and architectures for low-power design, more innovation for low-power testing will happen; in this respect, we believe that this book will serve as an inspiration for future research and development in the field.
Index

A
Active logic switching, 273
Adaptive scan, 14
Address decoder fault, 19
Ad hoc DFT methods, 7
Adjacency based TPG, 165–166
induced activity function, 166
Adjacent fill, 88
Alternating run-length code, 152
Always ON, 331
Assignment, 91
At-speed, 201
At-speed testing, 51
Automatic test equipment (ATE), 13, 19, 147, 178
Automatic test pattern generation (ATPG), 9, 16, 32, 66, 149, 230, 295

B
Background data sequence (BDS), 22
Bathtub curve, 2
Best primary input change (BPIC), 69
Bit-pair, 91
Bit-stripping, 84
Body biasing, 208, 229, 231
adaptive body bias (ABB), 229, 231
forward body bias (FBB), 229
reverse body bias (RBB), 232
Boundary register, 141
Boundary-scan cell (BSC), 24
Bounded adjacent fill (BA-fill), 101
Bridging fault, 6
Bridging fault models, 6
Broadcast-scan-based schemes, 14
Broad-side, 18
Built-in logic block observer (BILBO), 12
Built-in self test (BIST), 7, 148, 159, 178, 195, 229
control
centralized, 168–169
distributed, 168–169
test-per-clock, 116
test-per-scan, 116
Burn-in, 19, 228
Burn-in test, 41–42
Bus contention, 55

C
Capacitance based full-open fault model, 256
Capture conflict (C-conflict), 74–75
Capture cycle, 201
Capture mode, 10
Capture power, 17, 120
Capture-power-aware (CPA) selective encoding, 102
Capture-power reduction, 201–202
Capture-safe, 72–74
Capture switching activity (CSA), 70
Capture transition probability (CTP), 99
Cell stuck-at fault, 19
Cellular automata, 159
Characteristic path, 85
Characterization test, 41
C-impact, 99
Circuit under test (CUT), 1, 65, 232
Clock control cube (CCC), 77
Clock-disabling, 90
Clocked-scan design, 10
Clock gating, 122–125, 217, 274
Clock-gating-based test relaxation and X-filling (CTX-fill), 94
Clock gating control, 217
Clock sequence, 130–131
Coarse-grained clock gate, 287
Code-based schemes, 14
Common power format (CPF), 300
Compatible free bit set (CFBS), 104
Compatible PHS-fill, 103
Complementary metal oxide semiconductor (CMOS), 5, 204
Compressibility assurance, 104
Compressible JP-fill (CJP-fill), 104
Controllability, 7
Control pattern, 69
Core, 185
    predesigned, 176
    preverified, 176
Core access, 178
Core isolation, 178
Core test language (CTL), 23
Core test wrappers, 177–180
Core-under-test (CUT), 178
Coupling fault, 20
CRISTA, 219
Critical capture transition (CCT), 74, 97
Critical weight, 74
Cycle-accurate, 186

D
D-algorithm, 17
Data gating, 127, 274
Data line fault, 19
Data retention fault, 20
Defect, 2–3
Defective parts per million (DPPM), 318
Defect level, 3
Delay calibration, 237
Delay fault models, 7
Delay faults, 7
Design flows, 325–329
Design for manufacturability (DFM), 2, 22
Design for reliability (DFR), 2, 23
Design for testability (DFT), 3, 23, 230
Design for yield enhancement (DFY), 2, 23
Destructive read fault, 20
Detection conflict (D-conflict), 75
DFT for shift-power reduction, 200–201
DFT synthesis, 331–332
Diagnosis, 266–267
Dictionary code (fixed-to-fixed), 14
Direct generation, 82–83
Distribution-controlling X-identification (DC-XID), 86–87
Divide-and-conquer, 202
Domains crossing, 337–338
Dominant-AND, 6–7
Dominant bridging fault, 7
Dominant-OR, 6–7
Double-capture, 18
Droop, 45
    high frequency droop, 48–49
    low frequency droop, 46–47
    mid frequency droop, 47–48
Dual-speed LFSR, 163
    normal-speed LFSR, 163, 164
    slow-speed LFSR, 163, 164
Dual-Vth, 200–221
Dynamically justified clock gating, 291
Dynamic circuits, 236
Dynamic compaction, 14, 78
Dynamic power consumption, 274
Dynamic power dissipation, 37
    due to charging and discharging of load capacitor, 37–39
    due to short-circuit current, 39–40
Dynamic voltage and frequency scaling (DVFS), 218–219
Dynamic voltage scaling (DVS), 219, 227

E
Embedded deterministic test (EDT), 157
Enhanced Scan, 230
Entropy, 156
Error, 2
Essential fault, 84

F
Failure, 2
    rate, 2
Failure mode analysis (FMA), 4
False power, 185
Fault, 4
    activation, 17
    coverage, 3, 16
    models, 4
    propagation, 17
    simulation, 15–16
    type, 203
Fault-induced, 66
Fault list inferred switching (FLIS), 72
FF-silencing, 90
0-fill, 88, 101
1-fill, 88
Fine-grained clock gating, 283
First level hold (FLH), 233
First level supply gating (FLS), 231
Forced PHS-fill, 103
Free X-bit, 104
Frequency-directed run-length, 152
Functional testing, 5, 16
Index

G
Gated clock scheme, 166
Gate-delay fault, 7
Gated scan-chains, 149
Gate-level stuck-at fault model, 5
Gate sizing, 214, 226, 253
Gate tunneling leakage, 257
Gating of clock signals, 273
Glitches, 276
Global instantaneous toggle constraint (GITC), 72
Global peak power model, 185
Global power constraint, 187
Global toggle constraint (GTC), 72
Golomb code (variable-to-variable), 14
Golomb coding, 150
Graph partitioning, 134

H
Hardware Description Language (HDL), 224
Hierarchical design flows, 342
Hold scan, scan gadget, 233
Huffman code (fixed-to-variable), 14
Huffman coding, 151
Hyper edge, 134
Hyper graph, 134
  partitioning, 134

I
$\text{I}_{DDQ}$, 203
$\text{I}_{DDQ}$ testability, 223
$\text{I}_{DDQ}$ testing, 6
Idempotent coupling fault, 20
IEEE 1450, 342
IEEE 1801, 325
IEEE 1149.1 standard, 23
IEEE 1450.6 standard, 23
IEEE 1500 standard, 23, 179
IEEE Std 1500, 141
iFill, 98
Illinois scan, 158
Implied X-bit, 104
Incoming inspection, 42
Induced activity function, 107
Infant mortality, 3
Input control, 69
Input vector control (IVC), 219–220
Insertion
  ISO, 340–341
  LS, 340–341
Instantaneous switching, 283
Intellectual property, 2, 147

J
Justification-probability-based X-filling (JP-fill), 104

L
Launch-and-capture, 188
Launch-and-capture cycle, 186
Launch-on-capture (LOC), 18, 70
Launch-on-shift (LOS), 18, 70
Launch switching activity (LSA), 70
Leakage-aware full-open fault model, 256
Leakage power, 204
Level sensitive scan design (LSSD), 10, 233, 280
Level shifter, 261
Level shifter strategy, 326
LFSR-based decompressors, 157
LFSR reseeding, 157
Linear-decompression-based schemes, 14
Linear feedback shift registers (LFSRs), 13, 157
Line edge roughness (LER), 214
Line stuck-at fault model, 5
Local clock buffer, 124
Logic BIST, 159
Low-capture-power X-filling (LCP-fill), 97
Low-power dynamic compaction, 78–79
Low-power testing, 17
Low-transition random TPG (LT-RTPG), 165
LSSD scan design, 10

M
Manufacturing defects, 2
Manufacturing yield, 2
Manufacturing yield loss, 32, 54–57
March C-, 21
March D2pf, 22
March LR, 21
March S2pf-, 22
March X, 21
March Y, 21
MATS+, 21
MATS++, 21
Memory testing, 19–22
Minimum transition fill (MT-fill), 88
Minimum transition random X-filling (MTR-fill), 89
Modelling and test generation of resistive bridge, 244
Mode mapping, 335
Modified algorithmic test sequence (MATS), 20–21
Modular test, 176
Multi-capture, 77
Multi-mode DFT architecture, 346–348
Multiple clock domains, 202
Multiple input signature register (MISR), 13, 164
Multi-threshold CMOS (MTCMOS), 221
Multi-voltage, 319–320
Muxed-D scan design, 10
MUXed Scan, 277

N
Normal mode, 10

O
Observability, 7
On-die droop detector (ODD), 49
One-hot, 77
Online fault detection and correction, 4
On product clock generation (OPCG), 55, 281–282
Open defect distribution, 255
Operand isolation, 217–218
Ordering of test data, 193–194
Output response analyzer (ORA), 13
Over-test, 66

P
Packaging, 44–45
Parametric yield, 213
Parts per million (ppm), 4
Path-delay fault, 7
Pattern sensitivity fault, 20
Pattern suppression, 122
Peak power consumption, 161
Phase-locked loops, 281
Power, 33–40
droop, 175
estimation, 188–191
gating, 325–326
grid, 187, 200
manipulation, 191–194
model, 199
cycle-accurate, 186
peak power, 185
single-value, 185
two-value, 185
modeling of power and energy metrics, 57–59
power metrics, 57
Power-aware, 337
design-for-test, 176
test planning, 175, 183, 198
wrapper design, 192–193
Power-constrained test planning, 194–202
Power-constrained test scheduling, 195–198
Power-constraint, 177
Power constraint circuit (PCC), 69
Power consumption
dynamic part, 184
short-circuit power, 184
static part, 184
Power delivery, 31
issues during test, 43–50
Power distribution network (PDN), 187, 314–321
Power domains, 288, 334
annotation, 344
Power-induced, 66
Power island, 187
Power management unit (PMU), 298
Power specification format, 215
common power format (CPF), 224
low power coalition, 224
silicon industry initiative (Si2), 224
tool control language (TCL), 224
unified power format (UPF), 224–225
Power shut-off (PSO), 299
Power shut-off switches, 274
Power state table, 329, 348
Predictability, 345–346
Preferred fill, 92
Preferred Huffman symbol based X-filling (PHS-fill), 103
Preferred Huffman symbols (phss), 103
Preferred value, 93
Primary implication stack, 75
Primary input (PI), 68
Printed circuit board (PCB), 2
Probabilistic weighted capture transition count (PWT), 95
Process-tolerant design, 213
Production test, 41
Progressive match filling (PMF-fill), 92
Pseudo primary input (PPI), 68
Pseudo-random pattern generator (PRPG), 13
Pseudorandom patterns, 161
Q
Quiescent current, 213

R
Random access memories (RAMs), 19
Random dopant fluctuations (RDF), 214
Random fill, 17, 83
Random-pattern resistant, 161
RAZOR, 219, 234–235
Read disturb faults, 20
Read/write fault, 20
Redundant fault, 78
Regional instantaneous toggle constraint (RITC), 72
Region-based capture-safety checking, 72
Register-transfer level (RTL), 4
Reject rate, 3
Repeat fill, 88
Resistive bridge distribution, 244
Resistive open, 6
Resistive open fault model, 258
Response capture pulse, 70
Restoration implication stack, 75
Restoration implication stack list, 75
Retention
control, 329
strategy, 329
Re-use
ISO, 340–341
LS, 340–341
Reversible backtracking, 74–75
RL-Huffman encoding, 154
Rule of ten, 2
Run-length code (variable-to-fixed), 14
Scan cycle switching, 284
Scan design, 4, 7
partial, 125
power, 119
rules, 10
Scan forest, 136–138
Scan input (SI), 10
Scan insertion, 129
Scan-latch ordering, 154
Scan modeling, 343
Scan multiplexer, 203
Scan output (SO), 10
Scan partitioning, 168
non-uniform scan, 168
uniform scan, 168
3-valued weighted, 168
Scan replacement, 336
Scan router, 203
Scan segment, 129
inversion, 139
Scan structures mixing, 338
Scan tree, 136–138
double tree, 136–137
serial mode, 136
Scan-unload switching, 284
Scan wiring, 135
Selective encoding, 155, 156
Self-repair, 237–238
Self-test using MISR and parallel SRSG (STUMPS), 13, 124, 126, 161
Set covering, 127
Set-essential fault, 78
Shannon cofactoring, 222
Shift-in, 188
cycle, 186
transition, 87
Shift mode, 10
Shift-out, 188
cycle, 186
transition, 87
Shift power, 17, 120
Shift-power reduction, 200–201
Shift register latches (SRLs), 10
Shift register sequence generator (SRSG), 13
Shift transition probability (STP), 98
Signal probabilities, 161
S-impact, 98
Simulation-based testability analysis, 9
Single bit change (SBC), 108
Single event upsets (SEUs), 2
Single-value power model, 185
Six sigma, 4
Skewed clocking. See Staggered clocking
Skewed-load, 18
Sandia controllability/observability analysis program (SCOAP), 9
Scan architecting, 334
Scan architecture, 203
Scan-based logic built-in self-test (BIST), 4
Scan cell, 121
failure, 120
LS-S, 121
muxed-D, 121
polarity, 138
reordering, 167
suppressed, 127
Scan chain, 10, 176, 179
gating, 200
reordering, 338–340
Scan clustering, 133
Skewed clocking. See Staggered clocking
Skewed-load, 18
Small delay defect, 7
Smooother, 167
Space compactors, 15
Speed binning, 237
Stacking effect, 220
Staggered clocking, 131
Standard for embedded core test (SECT), 179
State coupling faults, 21
State retention, 336–337
State retention logic, 265
Static compaction, 79–81
Static power dissipation, 33–37
Static random access memory (SRAM), 214
Statistical design approach, 214
STAtistical Fault ANalysis (STAFAN), 9
Stimulus launch pulse, 70
Stress testing, 19
Structural testing, 5, 16
Stuck-at, 203
Stuck-at-0, 5
Stuck-at-1, 5
Stuck-open, 5
Stuck-short, 5
Supply gating, 221–222
Supply nets, 349
Switching activity, 185
Switching cycle average power (SCAP), 73
Switching time window (STW), 73
Synopsys liberty format (.lib), 225
Synthesis of clock gating, 276
System-on-chip (SOC), 32, 147, 176
  core, 176
  modular, 176
  non-modular, 176

T
Testability analysis, 8, 138
Testable unit, 179, 185
Test access mechanism (TAM), 24, 177, 178
Test access port (TAP), 24
Test application time, 177
Test bus, 177
Test clock (TCK), 24
Test compression, 4, 7, 13, 148, 283
Test cube, 17, 78
Test data in (TDI), 24
Test data out (TDO), 24
Test design rules, 332
Tester power supply (TPS), 32
Test hold, 124
Test infrastructure, 177
Test mode (TM), 10
Test model, 342
Test mode select (TMS), 24
Test mode stability, 333
Test pattern generator (TPG), 11
Test-per-clock BIST, 12
Test-per-scan BIST, 12
Test planning, 125–127, 183, 345–351
Test plan optimization, 198
Test point insertion (TPI), 161, 252
Test points, 7
Test power consumption, 175
Test power estimation, 188
Test protocol, 331
Test relaxation, 83–87
Test response analyzer, 159
Test scheduling, 168–169, 177, 178, 346, 348
Test sink, 178, 195
Test source, 178, 195
Test stimuli generator, 159
Test throughput, 52–53
Test vector
  inhibiting, 163
  ordering, 193
  reordering, 193
  selection, 162
  non-detecting vector, 162
  useful patterns, 162
Test wrapper, 140
T (toggle) flip-flop, 165
Thermal hotspot, 51–53
Threshold voltage, 214
Time compactors, 15
Toggle count (TC), 72
Toggle suppression, 127–128
Topology-based testability analysis, 9
Total weighted transition metric (TWTM), 89
Transistor-level stuck fault model, 5–6
Transition controllability, 67
Transition-delay, 203
Transition fault, 7, 20
Transition frequency, 167
Transition graph, 106
Transition observability, 67
Transition test generation cost, 67
Traveling salesman problem, 135

U
Under-test, 65
Unified power format (UPF), 300, 327–329
Useless patterns, 122
User power mode, 348–350
| V | Variation avoidance, 214 |
|   | Vector-essential fault, 78 |
|   | Vector inhibiting, 149 |
|   | Very-large-scale integration (VLSI), 1 |
|   | Virtual scan, 14 |
|   | Voltage and process variation, 266 |
|   | Voltage annotation, 343–344 |
|   | Voltage droop, 226 |
| W | Wearout, 2 |
|   | Weighted switching activity (WSA), 72 |
|   | Weighted transition, 80 |
|   | Weighted transitions metric (WTM), 151 |
|   | Wired-AND/wired-OR, 6 |
|   | Working life, 3 |
|   | Wrapped core, 177 |
|   | Wrapper, 23 |
|   | core access, 178 |
|   | core isolation, 178 |
|   | IEEE 1500, 179 |
|   | Wrapper boundary cells (WBCs), 24 |
|   | Wrapper boundary register (WBR), 24 |
|   | Wrapper bypass register (WBY), 24 |
|   | Wrapper chains, 179 |
|   | Wrapper instruction register (WIR), 24 |
|   | Wrapper parallel control (WPC), 24 |
|   | Wrapper parallel input (WPI), 24 |
|   | Wrapper parallel output (WPO), 24 |
|   | Wrapper parallel port (WPP), 24 |
|   | Wrappers, 178 |
|   | Wrapper serial control (WSC), 23–24 |
|   | Wrapper serial input (WSI), 23 |
|   | Wrapper serial output (WSO), 23 |
|   | Wrapper serial port (WSP), 23 |
| X | X-bit, 67 |
|   | X-bit limitation, 104 |
|   | X-classification, 104 |
|   | X identification (XID), 83, 84 |
|   | XOR compression, 14 |
|   | X-score, 95 |
|   | X-string, 88 |
| Y | Yield, 2 |
|   | yield loss, 176 |
| Z | Zero defect, 4 |